Lierda DB6L Series Hardware Design Manual

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Revision History

Document Version	Change date	Reviser	Reviewer	Change content
Rev1.0	23-09-25	LHL	YB	Initial Version

Safety Instructions

Users are responsible for complying with the relevant regulations regarding wireless communication modules and devices in other countries and specific regulations on the use environment. By following the following safety principles, personal safety can be ensured and help protect products and work environments from potential damage. Our company is not responsible for any losses resulting from customers' failure to comply with these regulations.

	Road safety comes first! When driving, please do not use handheld mobile devices unless they have a hands-free function. Please pull over before making a call!
	Please turn off your mobile electronic devices before boarding. The wireless function of mobile devices is prohibited from being turned on in the aircraft to prevent interference with the aircraft communication system. Ignoring this prompt may compromise flight safety and even violate the law.
	When in a hospital or healthcare facility, pay attention to any restrictions on the use of mobile terminal devices. RF interference can cause medical equipment to malfunction, so it may be necessary to turn off mobile terminal devices.
	Mobile terminal devices do not guarantee effective connection in all circumstances, such as when the mobile terminal device has no airtime or the SIM card is invalid. In the event of an emergency under these circumstances, please remember to use emergency calls, ensuring that your device is powered on and in an area with sufficient signal strength.
	Your mobile terminal device will receive and emit radio frequency signals when it is turned on, which may cause radio frequency interference when approaching a TV, radio, computer, or other electronic devices.
	Please keep mobile terminal devices away from flammable gases. When you are near gas stations, oil depots, chemical plants, or explosive operation sites, please turn off your mobile terminal device. Operating electronic devices in any potentially explosive environment poses a safety hazard.

Module selection for application

Serial number	Module model	Support frequency band	Dimensions (mm)	Module introduction
1	L-WFMDB6L-G5NN4	2.4 GHz ISM Band	12×12×2.6	\

目录

1 Introduction

The DB6L series module is a Wi-Fi 6 module that supports IEEE 802.11b/g/n/ax@2.4G and BLE 5.2 functions, supporting SDIO 2.0 interface. The module supports standard 20/40MHz bandwidth to ensure backward and network compatibility; it can be widely used in areas such as IPC, surveillance cameras, smart homes, security devices, dash cams, and smart access control.

Figure 1.1 Module Schematic

2 Product Overview

2.1 Key Features

Interface	LCC+ postage stamp hole
Wireless standard	IEEE 802.11b/g/n/ax+BLE5.2
Module packaging	12 mm × 12 mm × 2.6 mm
Operating voltage	3.0V~3.6V, typical value 3.3V
Working frequency band	2400~2483.5MHZ(2.4GHz ISM Band)
Operating temperature	-20 ~ +80℃
Storage temperature	-40 ~ +85℃
Communication interface	SDIO 2.0
Bandwidth	Support standard 20/40MHz bandwidth.
MAC	IEEE 802.11d/e/i/k/v/w

2.2 Product advantages

(1) Support IEEE 802.11b/g/n/ax@2.4G

(2) Support BLE 5.2

(3) Support STA, AP, and Wi-Fi Direct modes.

(4) Support WEP/WPA/WPA2/WPA3-SAE Personal, MFP band.

(5) Support Wi-Fi/BLE time-division multiplexing.

(6) Support SDIO 2.0 interface

(7) Support MU-MIMO, OFDMA

(8) Support Wi-Fi 6 TWT

2.3 Application Scenarios

- IPC, monitoring PTZ
- Smart home, security equipment
- Dashboard camera
- Smart access control

2.4 Function block diagram

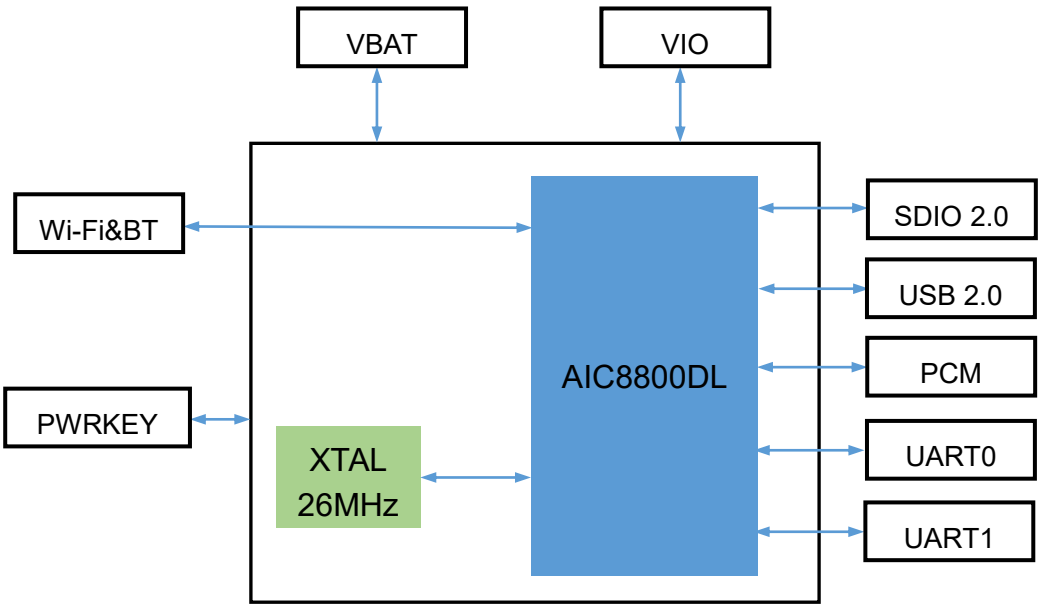


Figure 2.1 Functional Block Diagram

2.5 Pinout diagram

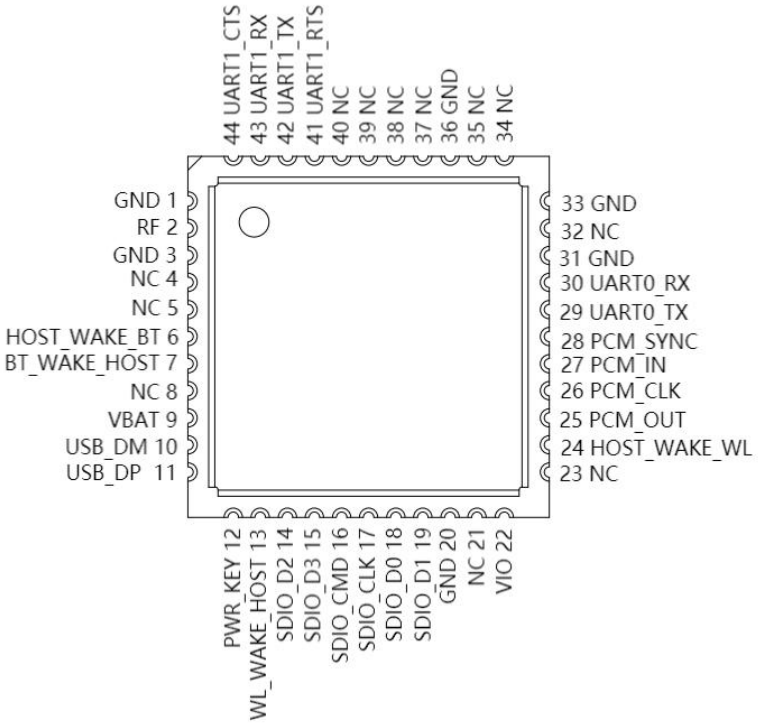


Figure 2.2 Pinout Diagram

2.6 Pin Description Table

Pins	Pin definition	I/O Type	Voltage	Function Description
1	GND	G	–	Ground
2	RF	ANT	–	2.4G Wi-Fi & BT Antenna
3	GND	G	–	Ground
4	NC	NC	–	NC pin, handle floating
5	NC	NC	–	NC pin, handle with floating
6	HOST_WAKE_BT	I	VIO	Wake up the pin, the master wakes up the BT function.
7	BT_WAKE_HOST	O	VIO	Wake-up pin, BT wake-up host function
8	NC	NC	–	NC pin, floating treatment
9	VBAT	P	3.3V	Power
10	USB_DM	I/O	–	USB DATA -
11	USB_DP	I/O	–	USB DATA +
12	PWR_KEY	I	VIO	Power on to enable pin. (Enabled: Pull up; Disabled: Pull down)
13	WL_WAKE_HOST	O	VIO	Wake up pin, Wi-Fi wake up host function
14	SDIO_D2	I/O	VIO	SDIO data line 2
15	SDIO_D3	I/O	VIO	SDIO data cable 3
16	SDIO_CMD	I/O	VIO	SDIO command/response
17	SDIO_CLK	I	VIO	SDIO clock signal
18	SDIO_D0	I/O	VIO	SDIO data line 0
19	SDIO_D1	I/O	VIO	SDIO data cable 1
20	GND	G	–	Ground
21	NC	NC	–	NC pin, handle floating
22	VIO	P	VIO	IO power supply, all IO level selection pins, support 1.8V and 3.3V

23	NC	NC	–	NC pin, handle floating
24	HOST_WAKE_WL	I	VIO	Wake up the pin, the main control wakes up the Wi-Fi function.
25	PCM_OUT	O	VIO	PCM data signal output
26	PCM_CLK	O	VIO	PCM clock signal
27	PCM_IN	I	VIO	PCM data signal input
28	PCM_SYN	O	VIO	PCM synchronization signal
29	UART0_TX	O	VIO	UART0 serial port transmit pin
30	UART0_RX	I	VIO	UART0 serial port receive pin
31	GND	G	–	GND
32	NC	NC	–	NC pin, floating treatment
33	GND	G	–	GND
34	NC	NC	–	NC pin, handle floating
35	NC	NC	–	NC pin, floating treatment
36	GND	G	–	GND
37	NC	NC	–	NC pin, handle floating
38	NC	NC	–	NC pin, handle floating
39	NC	NC	–	NC pin, handle floating
40	NC	NC	–	NC pin, handle floating
41	UART1_RTS	O	VIO	UART1 port RTS pin
42	UART1_TX	O	VIO	UART1 serial port transmission pin
43	UART1_RX	I	VIO	UART1 serial port receive pin
44	UART1_CTS	I	VIO	UART1 port CTS pin

Note

"P":POWER "I":INPUT "O":OUTPUT "G":GND

3 Characteristics of work

3.1 Power supply design

3.1.1 Power interface

VBAT pin is used to connect an external power supply, the interface description is as follows:

Table 3-1 Power Supply Pin Definitions

Pin number	Pin definition	Description	Minimum value V	Typical value V	Maximum value V
9	VBAT	Module power	3.0	3.3	3.6
22	VIO	IO level selection	-	1.8/3.3	-

The module power supply range is 3.0~3.6V, ensuring that the operating voltage is not lower than 3.0V. The power supply current requirement is not less than 500mA.

VIO is used to select the IO pin level, which determines the IO level based on the external supply voltage, supporting 1.8V/3.3V IO levels.

3.1.2 Power supply design

The DB6L module power pin is recommended to use 22uF and 0.1uF decoupling capacitors. The capacitors should be placed as close as possible to the VDD power pin. The power supply voltage range requirement is 3.0~3.6V. When using a 3.3V power supply, it is necessary to ensure that the supply voltage is not lower than 3.0V. The VDD pin is directly connected to the VDD33_PA pin of the internal chip of the module. This pin is used to power the Wi-Fi PA module circuit. When the maximum power is transmitted, VDD33_PA needs to have a power supply capacity to meet a peak current of 300mA, and the power ripple is recommended to be within 10mV to avoid excessive ripple causing RF performance degradation. The recommended power circuit is as follows:

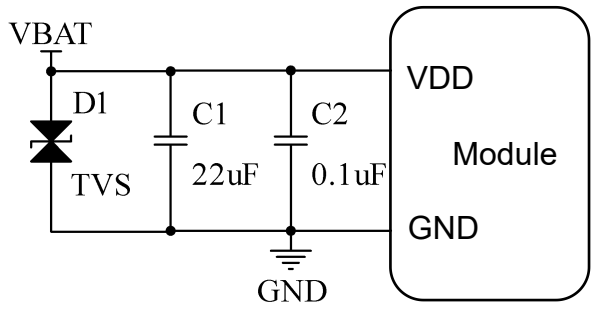


Figure 3.1 Power Supply Recommended Design

Note

For D1 TVS electrostatic protection, it is recommended to place TVS diodes for electrostatic protection.

3.1.3 Power-on timing sequence

When the power is applied to the VBAT pin of the DB6L module and reaches a stable state inside the module chip for a duration greater than 208ms, the power-on sequence of the module is as shown in the diagram below:

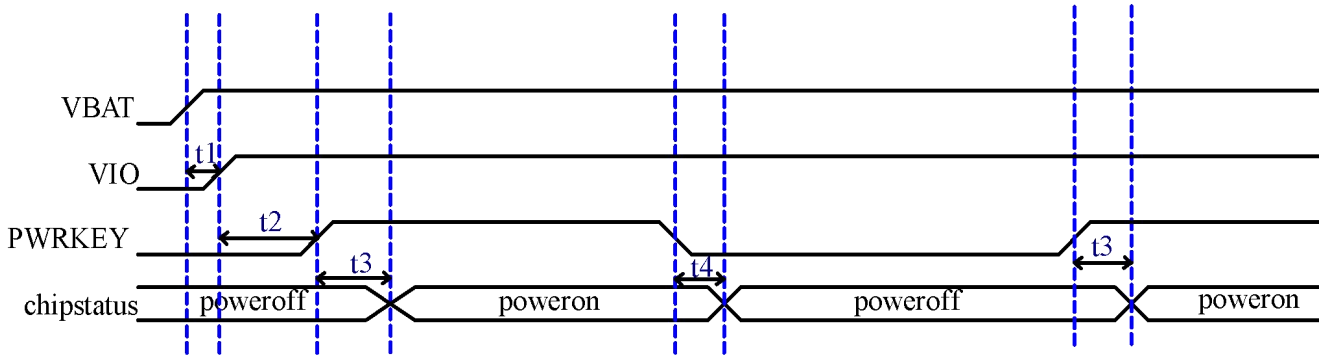


Figure 3.2 Power-on Sequence of the DB6L Module

t1: VIO power on ≥ VBAT power on

t2: Power on PWRKEY ≥ VIO power on + 200ms

t3: Power on initialization of the chip ≥ PWRKEY+8ms

t4: Pull down PWRKEY to power off the chip for ⩾6ms

4 Application Interface

4.1 SDIO interface

4.1.1 Description of SDIO interface

The SDIO interface is used for WIFI data transmission and firmware upgrade between the host controller. The interface description is as follows:

Table 4-1 SDIO Interface Pin Definitions

Pin number	Pin definition	Description	Note
14	SDIO_D2	SDIO data line 2	Pins support 1.8V/3.3V. PCB design uses two-layer board, connected in series with 50 Ω resistor; four-layer board, connected in series with 33 Ω resistor; The wiring length should be ⩽5 inches. SDIO0~3 pins, it is recommended to reserve pull-up resistors during design for convenient debugging and use.
15	SDIO_D3	SDIO data cable 3	
16	SDIO_CMD	SDIO commands/responses	
17	SDIO_CLK	SDIO clock signal	
18	SDIO_D0	SDIO data line 0	
19	SDIO_D1	SDIO data cable 1	

4.1.2 SDIO circuit reference design

The SDIO interface voltage level follows the VIO pin voltage level, supporting 1.8V/3.3V. The reference design for the SDIO interface is as follows:

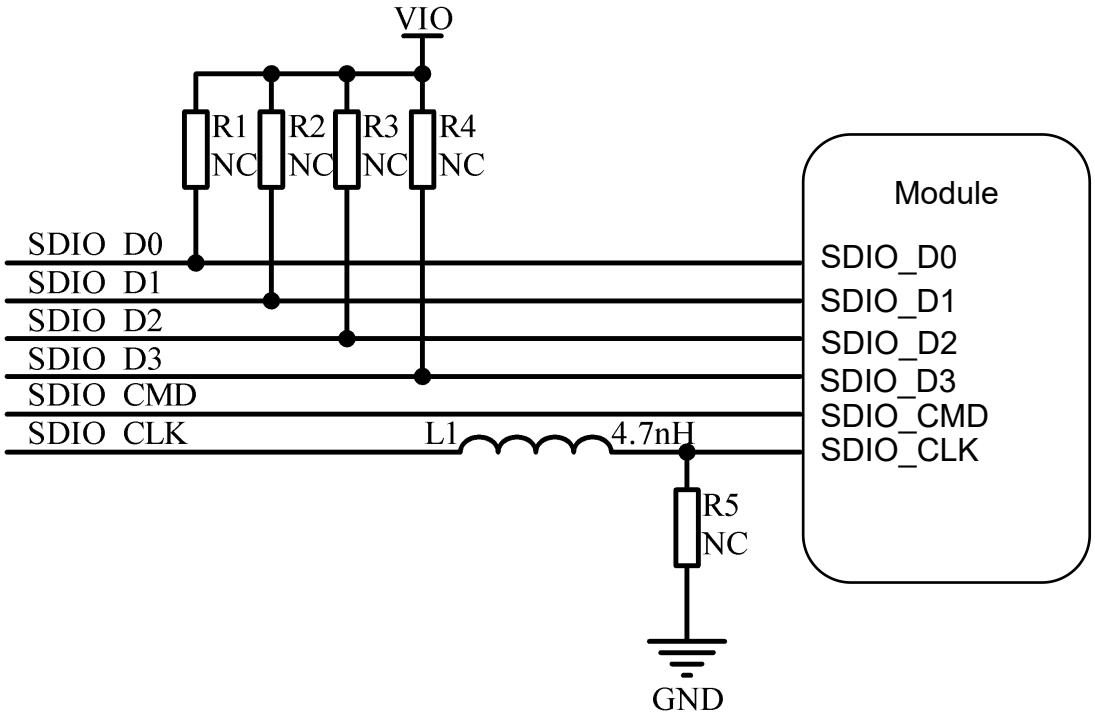


Figure 4.1 SDIO Reference Design

The SDIO interface voltage level is determined by the external power supply voltage of the VIO pin. The voltage level connected to the host control end needs to be consistent with the module end. If they are not the same, a level conversion circuit needs to be added between them.

The interface cabling recommendations are as follows:

(1) SDIO supports up to 50MHz, requiring layout and wiring to be far away from sensitive power, RF, and analog sections, and the trace length should be kept as short as possible, not exceeding 5 inches.

(2) The routing spacing of SDIO should strictly follow the 3W rule, which means keeping a distance of 3 times the line width between signals to avoid crosstalk between signals; the SDIO_CLK signal should be treated with a ground plane, the ground plane should be made as thick as possible, and ground vias should be placed on both sides of the routing.

(3) SDIO_CLK is connected to the main control end in series with inductance and to GND resistance to avoid SDIO_CLK affecting WIFI reception performance.

(4) SDIO_DATA(0~3) reserves one end of the pull-up resistor directly connected to the signal line, and the other end is connected to VIO. This can reduce signal reflection.

4.2 USB interface

4.2.1 Description of USB interface

The DB6L module supports the USB 2.0 interface, which is used for communication data transfer and firmware upgrade. The interface description is as follows:

Table 4-2 USB Interface Pin Definitions

Pin number	Pin definition	Description	Note
4	D-	USB differential data (-)	Differential impedance control is required during the design.
5	D+	USB differential data (+)	

4.2.2 USB circuit reference design

USB signals are differential high-speed signals. When designing, it is important to control the differential impedance and ensure equal length. Please refer to the design below:

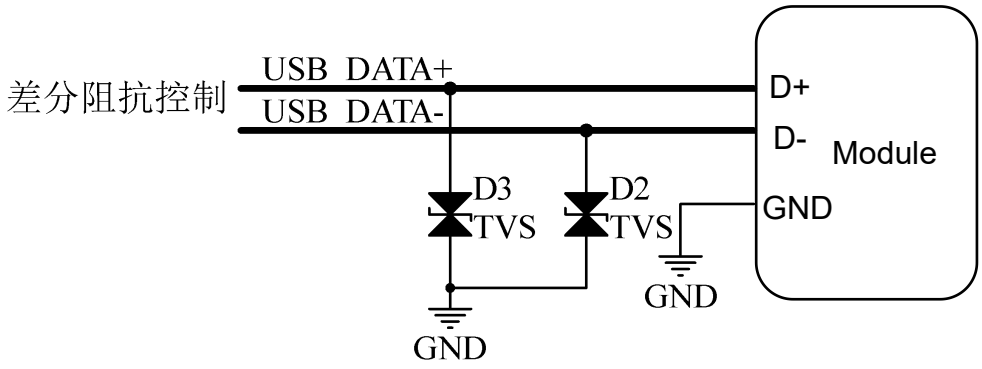


Figure 4.2 USB reference design

D2 and D3 are TVS diodes, used to prevent interference caused by hot-plugging of the USB interface, which may lead to abnormal operation of the internal circuit. When connected to an external USB connector, it is recommended to add TVS diodes and place them close to the USB interface. It is recommended to select protective devices with a

junction capacitance less than 0.6pF.

USB differential line routing considerations:

- Differential impedance control at 90 ohms ±15%;
- Common mode impedance is controlled at 30Ohm ± 30%, and ensure equal length;
- Cable Skew is less than 100ps, Cable Delay is less than 26ns;
- Grounding treatment is required around the routing, away from areas such as crystal oscillators, crystals, magnetic devices or equipment, and RF signals.

4.3 PCM interface

Voice data is transmitted through the PCM interface, and the interface level supports 1.8V/3.3V, which needs to be determined based on the external level of VIO. Pay attention to level conversion. The interface is specifically described as follows:

Table 4-3 PCM Interface Pin Definitions

Pin number	Pin definition	Description	Note
25	PCM_OUT	PCM data signal output	Pin direct connection, pay attention to VIO external voltage level, do you need a level conversion circuit
26	PCM_CLK	PCM clock signal	
27	PCM_IN	PCM data signal input	
28	PCM_SYN	PCM synchronization signal	

4.4 UART interface

The UART interface includes UART0 and UART1, where UART0 is used by default for LOG printing, and UART1 is used for BT data transmission between the main controller.

4.4.1 UART0 interface

UART0 interface is used for LOG printing by default, and can also be used for firmware burning and debugging, with a baud rate of 921600. The interface description is as follows:

Table 4-4 UART0 Interface Pin Definitions

Pin number	Pin definition	Description	Note

29	UART0_TX	UART0 serial port transmission pin	Pin direct connection, pay attention to VIO external voltage level, do you need a level conversion circuit
30	UART0_RX	UART0 serial port receive pin	

4.4.2 UART1 interface

BT data is transmitted between Lierda and the host through UART1, supporting flow control. The interface pin descriptions are as follows:

Table 4-5 UART1 Interface Pin Definitions

Pin number	Pin definition	Description	Note
41	UART1_RTS	UART1 port RTS pin	Pin direct connection, pay attention to VIO external voltage level, do you need a level conversion circuit?
42	UART1_TX	UART1 serial port transmission pin	
43	UART1_RX	UART1 serial port receive pin	
44	UART1_CTS	UART1 port CTS pin	

UART1_TX and UART1_RX are used for data transmission, UART1_RTS and UART1_CTS are used for flow control, the serial port baud rate is 921600.

4.5 PWR_KEY enable interface

PWR_KEY is the enable pin, PWR_KEY pin has a 200K pull-down resistor and a 47K pull-up resistor internally, pulling up to VBAT pin. Pulling the pin high enables it, pulling it low shuts down. The pin threshold values are as follows:

Table 4-6 PWR_KEY threshold

PWR_KEY	Voltage level state	Threshold
High	0->1	1.125V
Low	1->0	0.625V

Pull up inside the module, power off the module by pulling down the PWR_KEY pin. The reference design is as follows:

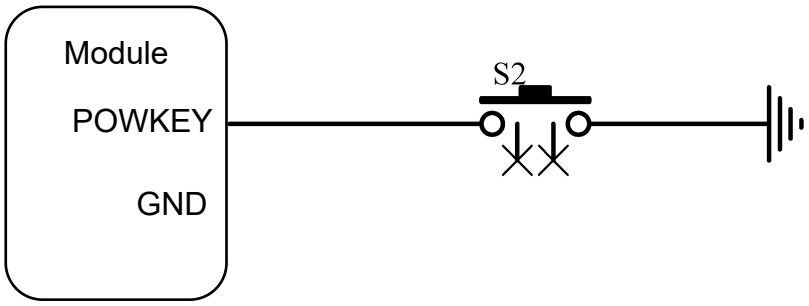


Figure 4.3 Reference Design of POW_KEY Circuit

4.6 VIO pin level selection interface

The VIO pin can be connected to a 1.8V/3.3V voltage power supply to determine the IO level. Apart from the USB interface, all GPIO levels of the module follow the level of the VIO pin. The maximum driving current for a single GPIO is 10mA. When VIO is at different levels, the threshold values for the corresponding GPIO pins are as follows:

Table 4-7 VIO Voltage Thresholds

VIO	Voltage level state	GPIO threshold
1.8V	0->1	1.18V
1.8V	1->0	0.59V
3.3V	0->1	2.62V
3.3V	1->0	0.44V

5 Radio Frequency Characteristics

5.1 Antenna Interface

Table 5-1 Antenna Interface Definition

Pin number	Pin definition	I/O type	Description	Note
2	RF	ANT	2.4G Wi-Fi & BLE antenna interface	50Ω characteristic impedance

5.2 Wi-Fi performance

Table 5-2 Wi-Fi Performance Parameters

Performance	Description	
Wireless standards	IEEE 802.11b/g/n/ax(@2.4GHz),Wi-Fi compliant	
Working frequency	2.400GHz ~ 2.4835GHz (2.4GHz ISM Band)	
Channel	2.4GHz：Ch1 ~ Ch13	
Modulation method	802.11b	DQPSK,DBPSK,CCK
	802.11g/n：OFDM	64-QAM,16-QAM,QPSK,BPSK
	802.11ax：OFDMA	1024-QAM,256-QAM,64-QAM, 16-QAM,QPSK,BPSK
Transmit Power	802.11b/1Mbps	20dBm ± 2dB@EVM ≤ -10.5dB
	802.11b/11Mbps	20dBm ± 2dB@EVM ≤ -15.5dB
	802.11g/6Mbps	20dBm ± 2dB@EVM ≤ -5dB
	802.11g/54Mbps	16dBm ± 2dB@EVM ≤ -25dB
	802.11n/MCS0(20/40M)	20dBm ± 2dB@EVM ≤ -5dB
	802.11n/MCS7(20/40M)	16dBm ± 2dB@EVM ≤ -27dB
	802.11ax/MCS0(20/40M)	20dBm ± 2dB@EVM ≤ -5dB
	802.11ax/MCS9(20/40M)	16dBm ± 2dB@EVM ≤ -32dB
	802.11ax/MCS11(20/40M)	15dBm ± 2dB@EVM ≤ -35dB
Frequency tolerance	±20ppm	
Receive Sensitivity	1Mbps	PER@-96.5dBm,typical

(11b,20MHz) @8% PER	11Mbps	PER@-88dBm,typical
Receive Sensitivity (11g,20MHz) @10% PER	6Mbps	PER@-93dBm,typical
	54Mbps	PER@-75.5dBm,typical
Receive Sensitivity (11n,20MHz) @10% PER	MCS=0	PER@-91.5dBm,typical
	MCS=7	PER@-73dBm,typical
Receive Sensitivity (11n,40MHz) @10% PER	MCS=0	PER@-88.5dBm,typical
	MCS=7	PER@-70dBm,typical
Receive Sensitivity (11ax,20MHz) @10% PER	MCS=0	PER@-91.5dBm,typical
	MCS=9	PER@-66dBm,typical
Receive Sensitivity (11ax,40MHz) @10% PER	MCS=0	PER@-88.5dBm,typical
	MCS=9	PER@-63.5dBm,typical

5.3 BT performance

The DB6L module supports BLE mode.

5.3.1 BLE mode

Table 5-3 BT performance parameters

Performance	Description
Bluetooth standard	BLE5.2
Working frequency	2.402GHz ~ 2.480GHz
Channel	LE：Ch0 ~ Ch39
Modulation method	GFSK
Transmit power	0.2~12.2dBm
Sensitivity @ PER=30.8% for LE(1Mbps)	-100.5dBm
Sensitivity @ PER=30.8% for LE(2Mbps)	-97.5dBm
sensitivity, @ PER=30.8% for LE Coded (S=2)	-105.5dBm
sensitivity, @ PER=30.8% for LE Coded (S=8)	-110.5dBm

Maximum input level	0dBm

5.4 Reference design

When using the DB6L module, a π -type matching circuit needs to be reserved between the RF antenna interface of the module and the antenna interface of the baseboard. It is recommended to use the antenna matching circuit with the initial parameters as shown in the figure below:

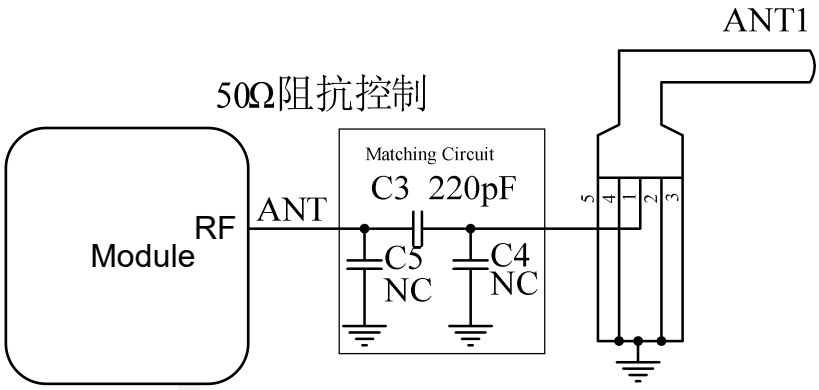


Figure 5.1 Antenna Reference Design Circuit

C3 defaults to using a 220pF capacitor or a 0 Ω resistor, while C4 and C5 are not populated for matching reserve, and their final values will be determined based on actual tuning results.

The routing of the antenna interface to the mainboard antenna must ensure a 50 Ω impedance control, the routing should be as short as possible, without vias, and avoiding sharp angle turns. Place GND vias around the RF routing. As shown in the figure 5.2 below:

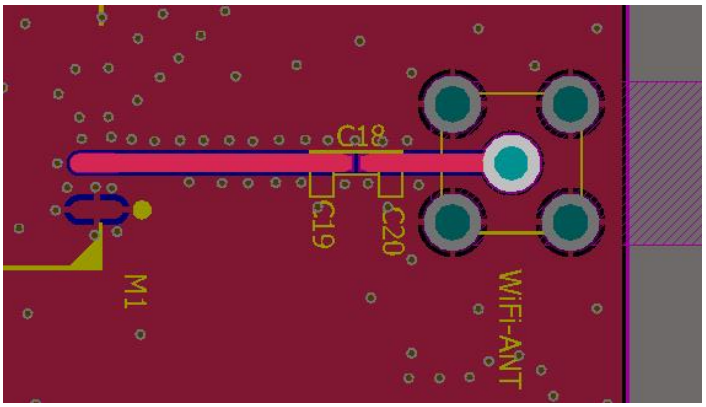


Figure 5.2 Impedance line of the bottom plate

The relationship between board thickness and line width and spacing can be referred to:

Recommended values for FR4 double-sided board (H=board thickness, W=line width, D=spacing between trace and copper pour)

- H=1.0mm，W=0.8mm，D=0.2mm
- H=1.0mm, W=1.0mm, D=0.254mm (recommended)
- H=1.2mm, W=1.0mm, D=0.2mm (recommended)
- H=1.6mm, W=1.0mm, D=0.2mm (recommended)

For the π-type matching circuit, to avoid introducing additional parasitic parameters that may affect the difficulty of debugging, it is recommended to place it as shown in the figure below:

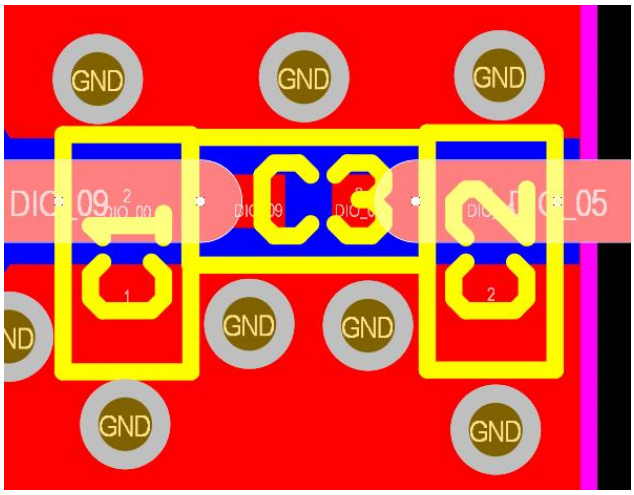


Figure 5.3 Matching circuit LC placement.

6 Electrical performance and reliability

6.1 Rated power value

Parameters	Description	Minimum value	Typical value	Maximum value	Unit
V_{DD}	Power Supply	3.0	3.3	3.6	V

6.2 Power consumption

Description	Test conditions	Maximum value	
		@TX(mA)	@RX(mA)
Wi-Fi data transmission	802.11b, 11Mbps @ 20dBm, duty cycle 80%	247	31
	802.11g, 54Mbps @ 16dBm, duty cycle 50%	130	32
	802.11n, HT20, MCS7 @ 16dBm, duty cycle 50%	127	31
	802.11n, HT40, MCS7 @ 16dBm, duty cycle 40%	98	32
	802.11ax, HE20, MCS11 @ 15dBm, duty cycle 50%	104	32
	802.11ax, HE40, MCS11 @ 15dBm, duty cycle 40%	92	40
BT data transmission	BLE @1M default power	120	62
	BLE @2M default power	80	64
	BLE @S=8 default power	145	65
	BLE @S=2 default power	110	66
Power-off state	PWR_KEY pulled low	72uA	

6.3 Digital logic level characteristics

Parameters	Description	Minimum value	Typical value	Maximum value	Unit
V_{IL}	CMOS Low Level Input Voltage	0	/	0.3*VDD	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDD	/	VDD	V

V_{TH}	CMOS Threshold Voltage	/	0.5*VDD	/	V

6.4 Static electricity protection

Parameters	Description	Minimum value	Typical value	Maximum value	Unit
V_{ESD}	VDD PIN ESD	/	1	/	KV
	ANT PIN ESD	/	1	/	KV

6.5 Work and storage temperature

Parameters	Description	Minimum value	Typical value	Maximum value	Unit
T_A	Operating temperature	-20	/	+80	℃
$T_{Storage}$	Storage temperature	-40	/	+85	℃

7 Mechanical dimensions

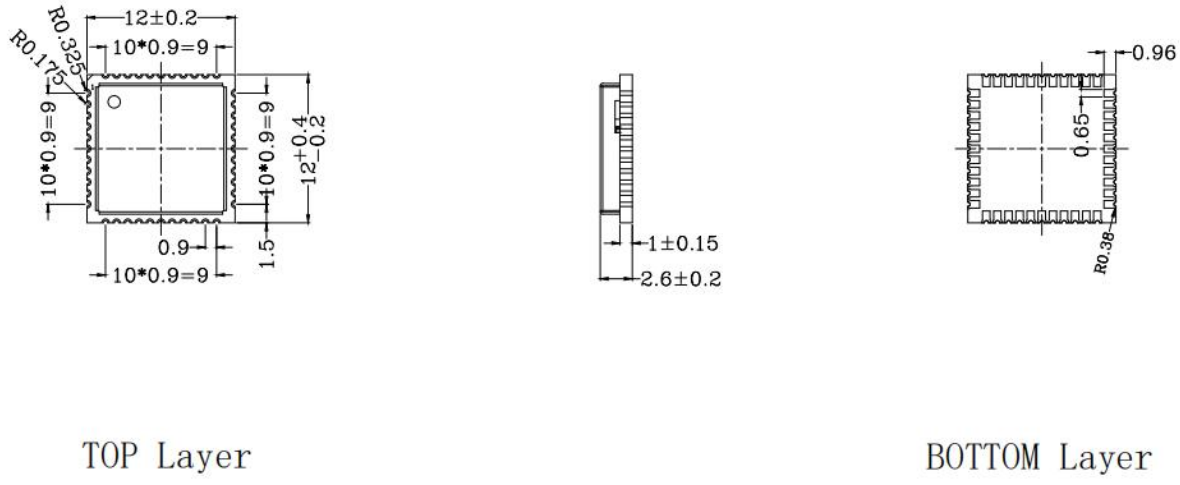


Figure 7.1 Module Outline Dimensions Figure

8 Production and packaging information

8.1 Production welding

8.1.1 Production Guide

It is recommended to use SMT machine for the stamp mouth sealing module assembly, and the patch should be completed within 24 hours after unpacking. Otherwise, it is necessary to re-vacuum package to avoid moisture causing poor patch.

If there is a humidity indicator card inside the package, it is recommended to determine whether the module needs to be baked based on the indication of the humidity card. The conditions for baking are as follows:

Baking temperature: 125°C ± 5°C;

The alarm temperature is set to 130℃;

After cooling to below 36°C under natural conditions, SMT mounting can be performed.

If the unpacking time exceeds 3 months, special attention should be paid to whether the product is damp, because the PCB immersion gold process, exceeding 3 months may cause oxidation of the solder joints, which may lead to problems such as false soldering and missed soldering during SMT.

To ensure the qualification rate of reflow soldering, it is recommended to randomly select 10% of the products for visual inspection and AOI inspection during the first placement, to ensure the rationality of furnace temperature control, component adsorption method, and placement method.

Operators at each workstation throughout the production process must wear antistatic gloves.

8.1.2 Module placement requirements on the baseboard

It is suggested that the green oil thickness of the bottom plate module position should be less than 0.02mm to avoid excessive thickness, which may prevent the spacer module

from effectively contacting the solder paste and affecting the welding quality. In addition, it is necessary to ensure that no other components are arranged within 2mm around the interface board module position to facilitate the maintenance of the module.

8.1.3 Steel mesh opening design

The selection principle of the thickness of the steel mesh on the substrate is generally based on the comprehensive consideration of the packaging types of the components inside the board, and the following requirements need to be focused on:

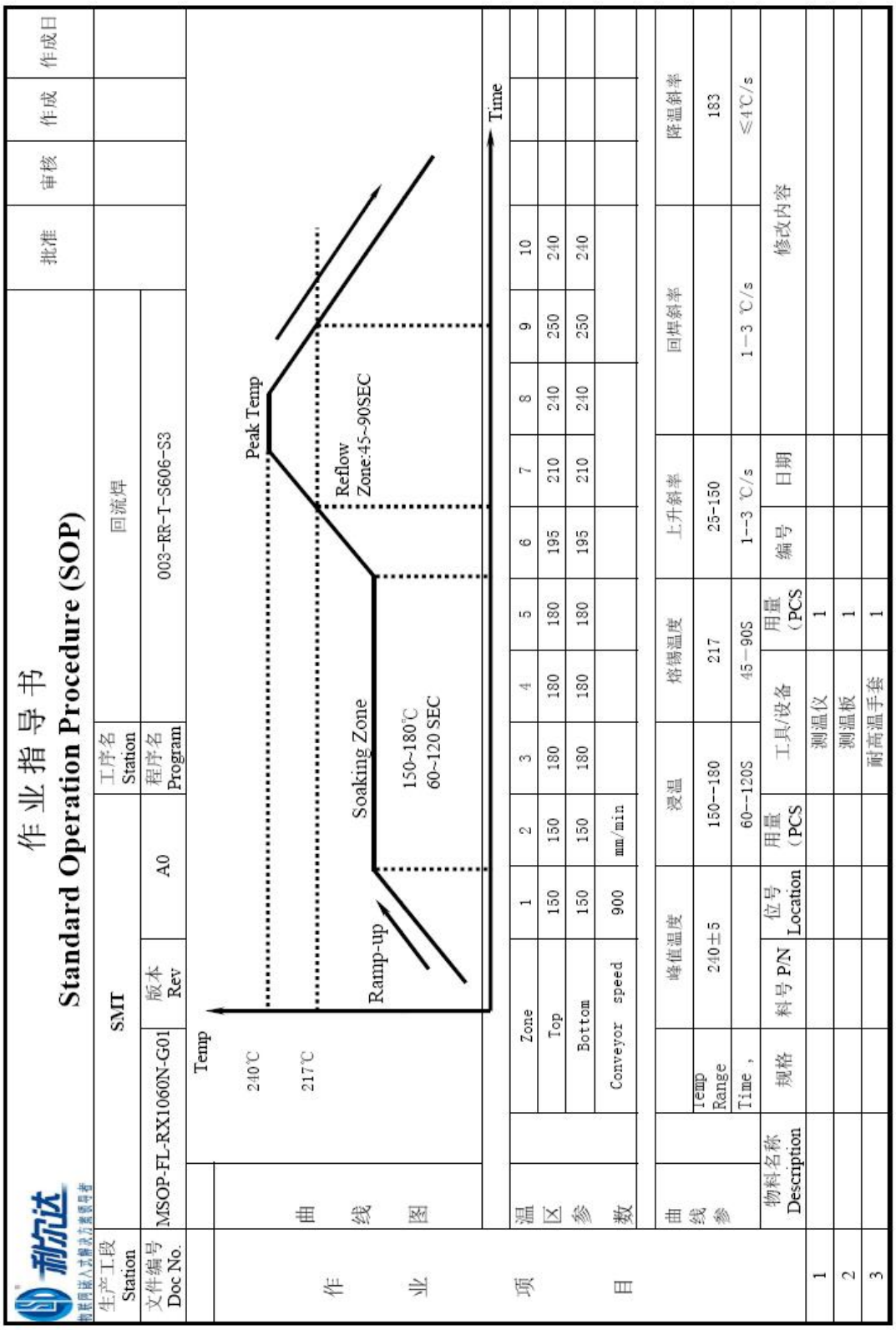
The module solder pad position can be locally thickened to 0.15-0.20mm to avoid solder voids.

8.1.4 Production Notes

- During the production process, all operators must wear antistatic gloves.
- Baking should not exceed the specified baking time.
- Do not add explosive, flammable, or corrosive substances during baking;
- During baking, the modules should be placed in high-temperature trays to ensure air circulation between the modules.
- When baking, make sure to close the oven door to ensure the oven is sealed and prevent temperature leakage.
- Try not to open the oven door while it is running. If you must open it, try to shorten the time the door is open as much as possible.
- After baking, wait for the module to cool naturally to below 36°C before wearing electrostatic gloves to avoid scalding.
- When operating, be sure to prevent the bottom of the module from getting wet or contaminated.

8.1.5 Reflow soldering operation guidance

This assignment guide is only suitable for lead-free operations and is for reference only.



作业指导书
Standard Operation Procedure (SOP)

生产工段 Station	SMT		工序名 Station	回流焊	批准	审核	作成	作成日
文件编号 Doc No.	MSOP-FL-RX1060N-G01	版本 Rev	A0	程序名 Program	003-RR-T-S606-S3			

作业曲线图

项目

温区参数	Zone	1	2	3	4	5	6	7	8	9	10
	Top	150	150	180	180	180	195	210	240	250	240
	Bottom	150	150	180	180	180	195	210	240	250	240
	Conveyor speed	900	mm/min								

曲线参数		峰值温度	浸温	熔锡温度	上升斜率	回焊斜率	降温斜率
	Temp Range	240±5	150--180	217	25-150	183	
	Time ,		60--120S	45--90S	1--3 ℃/s	1--3 ℃/s	≤4℃/s

	物料名称 Description	规格	料号 P/N	位号 Location	用量（PCS	工具/设备	用量（PCS	编号	日期	修改内容
1						测温仪	1			
2						测温板	1			
3						耐高温手套	1			

Figure 8.1 Reflow Soldering Operation Manual

8.2 Packaging specifications

8.2.1 Packaging method

Model	Packaging method	Carton (PCS)	Minimum packaging quantity (PCS)	Number of coils per box
L-WFMDB6L-G5NN4	Roller tape	6500	1300	5

8.2.2 Dimensions of the tape and product orientation

Schematic diagram of the placement orientation of the roll belt packaging module:

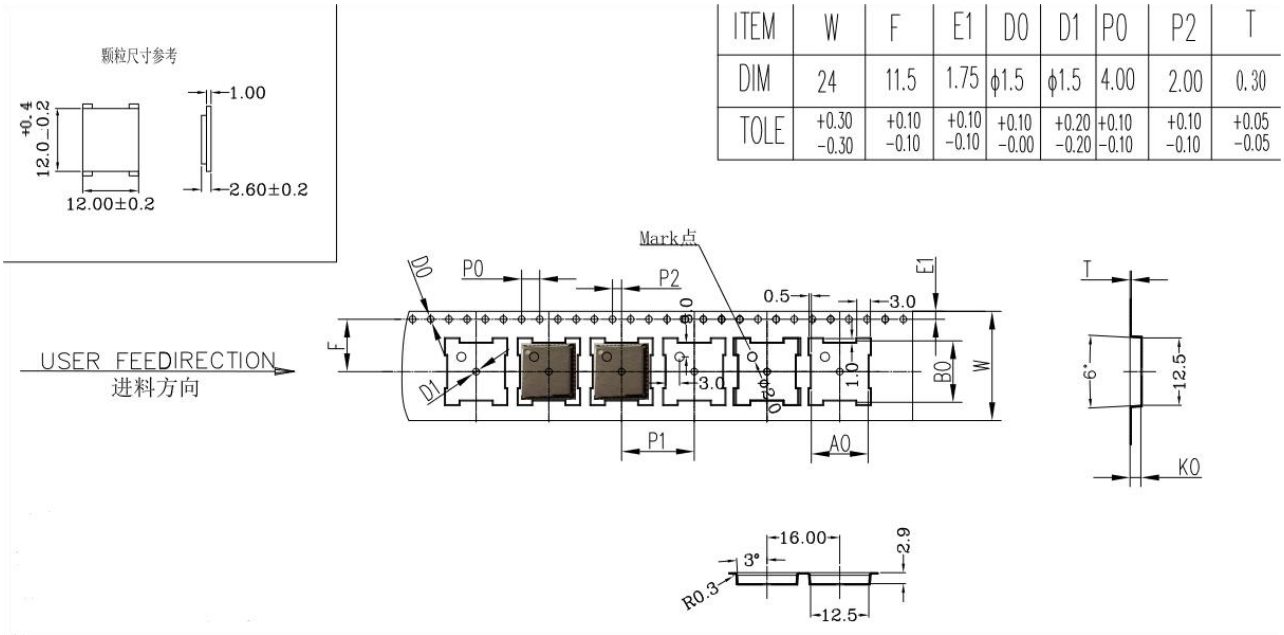


Figure 8.2 Tape Dimensions and Product Orientation