Lierda NE26U-CN Module Hardware Design Manual

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Revision History of the Document

Document Version	Change date	Reviser	Reviewer	Change content
Rev1.0	23-07-19	YY、BX	XL	Initial version
Rev1.1	24-08-01	YY、BX	XL	Optimize pinout diagram, update some content
Rev1.2	25-04-25	YY、BX	XL	Standardization optimization of documents

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	Safety first on the road! Do not use handheld mobile devices while driving unless they have hands-free functionality. Please pull over before making a call!
	Please turn off your mobile devices before boarding. The wireless function of mobile devices is prohibited from being turned on in the aircraft to prevent interference with the aircraft communication system. Ignoring this prompt may jeopardize flight safety and even violate the law.
	When in a hospital or healthcare facility, pay attention to any restrictions on the use of mobile terminal devices. RF interference can cause medical equipment to malfunction, so it may be necessary to turn off mobile terminal devices.
	Mobile terminal devices do not guarantee effective connection in all situations, such as when there is no phone credit or the SIM card is invalid. In case of emergency under the above circumstances, please remember to use emergency calls, and ensure that your device is powered on and located in an area with sufficient signal strength.
	Your mobile terminal device will receive and emit radio frequency signals when it is powered on, which may cause radio frequency interference when it is close to a TV, radio, computer, or other electronic devices.
	Please keep mobile terminal devices away from flammable gases. When you are near gas stations, oil depots, chemical plants, or explosive operation sites, please turn off your mobile terminal device. Operating electronic devices in any potentially explosive hazardous area poses a safety risk.

Module selection for application

Serial number	Module model	Characteristic Symbol	Support frequency band	Dimensions (mm)	Module introduction
1	NE26U-CN		WCDMA/LTE/NR	30*41.1*2.85	5G standard module

Content

1 Introduction

This document defines the hardware application specification of the Lierda Group's NE26U-CN 5G module, describing its hardware interfaces, electrical characteristics, application methods, and mechanical specifications.

This document can help users quickly understand the hardware interface specifications, electrical, mechanical characteristics, and other related information of the module. Combined with other corresponding documents, users can quickly master the application methods of the 5G module.

2 Product Overview

Lierda NE26U-CN 5G Sub-6GHz series module is based on the UNISOC V510 platform, supporting 5G standalone (SA) and non-standalone (NSA) networks, meeting the frequency band requirements of the four major domestic operators, and supporting LTE and WCDMA network standards.

The NE26U-CN module uses an LGA interface, with dimensions of 30*41.1*2.85mm, making it easy to install and helping customers quickly iterate towards 5G Rel-15, ensuring rapid project implementation.

The NE26U-CN module supports embedded systems such as Linux, Windows, and Android, and can provide voice functions to meet different application scenarios.

The NE26U-CN module is a surface-mount module with a total of 288 LGA pins.

NE26U-CN module is an industrial-grade module, only suitable for industrial and commercial applications.

The NE26U-CN module can be applied in the following terminal scenarios:

- Remote monitoring equipment
- Intelligent measuring equipment
- Wireless CPE
- Smart TV
- Wireless router and switch
- Outdoor live broadcasting equipment
- Other wireless terminal devices

2.1 Frequency bands and functions

The frequency bands supported by the NE26U-CN module are as shown in the table below:

Table 2-1 Description of Frequency Bands Supported by Lierda NE26U-CN Module

Frequency band	Launch	Receive
WCDMA Band 1	1920MHz-1980MHz	2110MHz-2170MHz
WCDMA Band 5	824MHz-849MHz	869MHz-894MHz
WCDMA Band 8	880MHz-915MHz	925MHz-960MHz
FDD LTE Band 1	1920MHz-1980MHz	2110MHz-2170MHz
FDD LTE Band 3	1710MHz-1785MHz	1805MHz-1880MHz
FDD LTE Band 5	824MHz-849MHz	869MHz-894MHz
FDD LTE Band 8	880MHz-915MHz	925MHz-960MHz
TDD LTE Band 34	2010MHz-2025MHz	2010MHz-2025MHz
TDD LTE Band 38	2570MHz-2620MHz	2570MHz-2620MHz
TDD LTE Band 39	1880MHz-1920MHz	1880MHz-1920MHz
TDD LTE Band 40	2300MHz-2400MHz	2300MHz-2400MHz
TDD LTE Band 41	2496MHz-2690MHz	2496MHz-2690MHz
NR n1	1920MHz-1980MHz	2110MHz-2170MHz
NR n5	824MHz-849MHz	869MHz-894MHz
NR n8	880MHz-915MHz	925MHz-960MHz
NR n28	703MHz-748MHz	758MHz-803MHz
NR n41	2496MHz-2690MHz	2496MHz-2690MHz
NR n77	3300MHz-4200MHz	3300MHz-4200MHz
NR n78	3300MHz-3800MHz	3300MHz-3800MHz
NR n79	4400MHz-5000MHz	4400MHz-5000MHz

2.2 Key Features

NE26U-CN module adopts 3GPP Rel-15 technology, which can meet the urgent needs of precise load control in the power industry, real-time control in industrial manufacturing, and multi-vehicle coordination in warehousing and logistics industries. The table below shows the main features of the NE26U-CN module.

Table 2-2 Main Characteristics of Lierda NE26U-CN Module

Type	Description
Encapsulation	LGA
Physical properties	Dimensions: 30*41.1*2.85mm Weight: about 8g
Working frequency band	5G SA：n1/n5/n8/n28/n41/n77/n78/n79 5G NSA：n41/n78/n79 LTE FDD：B1/B3/B5/B8 LTE TDD：B34/B38/B39/B40/B41 WCDMA：B1/B5/B8
Transmission rate (theoretical value)	SA DL：2Gbps；UL：1Gbps NSA DL：2.2Gbps；UL：575Mbps LTE DL：600Mbps；UL：150Mbps WCDMA DL：384kbps；UL：384kbps DC-HSPA+：DL 42.2Mbps HSUPA：UL 11Mbps
Transmit power	WCDMA Frequency Band: Class 3 (24dBm +1.7/-3.7dB) LTE band: Class 3 (23dBm ±2.7dB) 5G NR n1/n5/n8/n41：Class 3(23dBm ±2.7dB) 5G NR n28：Class 3(23dBm +2.7/-3.2dB) 5G NR n77/n78/n79：Class 3(23dBm +2.7/-3.7dB) 5G NR n41/n77/n78/n79 HPUE：Class 2 (26dBm +2.7/-3.7dB)
WCDMA features	Support 3GPP R9 DC-HSDPA, HSDPA, HSUPA, HSPA+, and WCDMA. Support QPSK, 16QAM, 64QAM modulation. Maximum transmission rate (theoretical value): DC-HSDPA: 42.2Mbps (downlink speed) HSUPA: 11Mbps (uplink speed) WCDMA: 384kbps (downlink speed) / up to 384kbps (uplink speed)
LTE features	Maximum support: 3CC downlink / 2CC uplink

Type	Description
	Downlink: Cat 12/Uplink: Cat 13 Support 1.4/3/5/10/15/20 MHz RF bandwidth. Support uplink QPSK, 16QAM, 64QAM modulation schemes. Support QPSK, 16QAM, 64QAM, 256QAM modulation schemes downstream. Support downlink 2×2 MIMO. Maximum transmission rate (theoretical value): LTE: 600Mbps (downlink speed) / 150 Mbps (uplink speed)
5G NR features	Support 3GPP Release-15. Support uplink 256QAM modulation scheme and downlink 256QAM modulation scheme. n1/n41/n77/n78/n79 support downlink 4×4 MIMO N41/N77/N78/N79 support uplink 2×2 MIMO. Support SCS 15kHz and 30kHz. Support the working modes of SA and NSA. Support Option 3x, 3a, 3 and Option 2 Maximum transmission rate (theoretical value, related to network configuration and heat dissipation environment): NSA: 2.2 Gbps (average downlink speed) / 575 Mbps (average uplink speed) SA: 2 Gbps (average downlink rate) / 1 Gbps (average uplink rate)
Operating voltage range	DC 3.3V ~ 4.3V (typical value 3.8V)
Application temperature range	Operating Temperature: -30 ~ +75° C Operating Temperature: -40 ~ +85° C Storage Temperature: -40 ~ +90° C
AT command	Reference the AT Command Manual Design Document for NE26U-CN.
USB interface	USB 2.0 interface, with a maximum speed of up to 480Mbps. USB 3.0 interface, with a maximum transfer rate of up to 5Gbps.
UART Interface	Main serial port: Used for data transmission and AT commands Debug serial port: partial log output
(U)SIM interface	2 standard SIM interfaces (Class B and Class C) Support dual SIM single standby.
PCM and I2S interfaces	PCM and I2S each have one interface. Support extending Codec or SLIC.
SPI interface	Implement SLIC function with PCM interface.

Type	Description
I2C interface	The maximum speed can reach 3.4Mbps.
PCIe interface	Compliant with PCI Express Base Specification Revision 2.0, the transmission rate can reach 5Gbps.
B code output interface	B code output interface, used for external device timing synchronization.
Control Indication Interface	PWRKEY (Low-Level Power On) RESET# (Low-level reset) W_DISABLE# (Flight Mode Control) STATUS (Operating status indicator) NET_MODE (Network Status Indicator) NET_STATUS (Network Status Indicator) SLEEP_IND (Sleep Status Indicator)
Antenna Interface	ANT0/ANT1/ANT2/ANT3
Network Protocol	PPP/RNDIS/ECM TCP/IP HTTP/MQTT/FTP
Drive	Linux Windows XP/7/8/10 Andriod
AT	Commands defined in 3GPP TS 27.007 and 3GPP TS 27.005. Lierda self-developed AT commands.
FOTA	Support
OneNET	Support
CTWing	Support
Certification	CCC/SRRC/NAL/ROHS/Operator Certification* (Telecom/Unicom/Mobile)

Note

*Under development

2.3 Function Block Diagram

The following diagram introduces the main functions of the NE26U-CN module: power management, baseband section, memory, RF function blocks, peripheral interfaces.

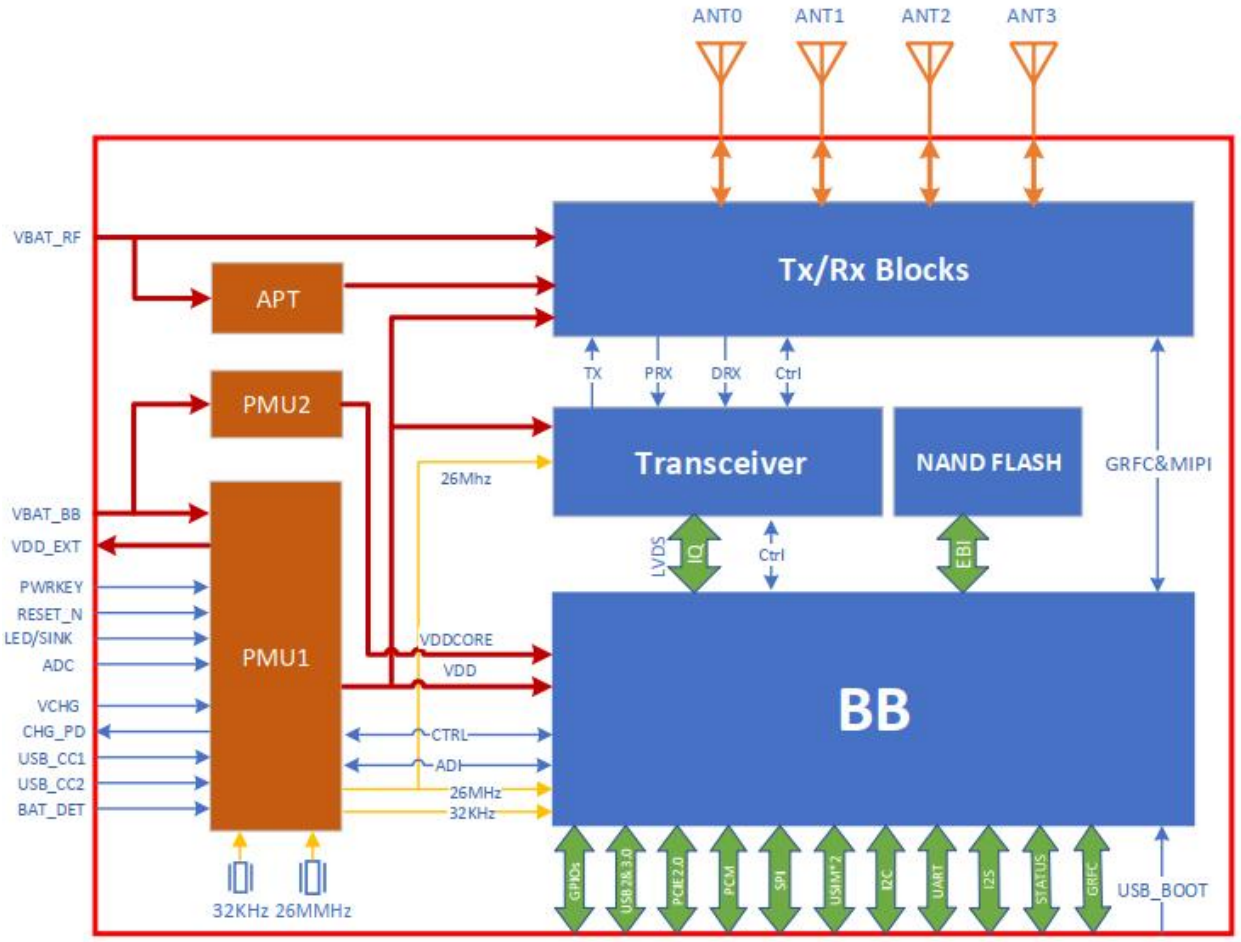


Figure 2.1 Hardware Block Diagram of NE26U-CN Module

2.4 Pinout diagram

The following is the pin assignment diagram for NE26U-CN interface.

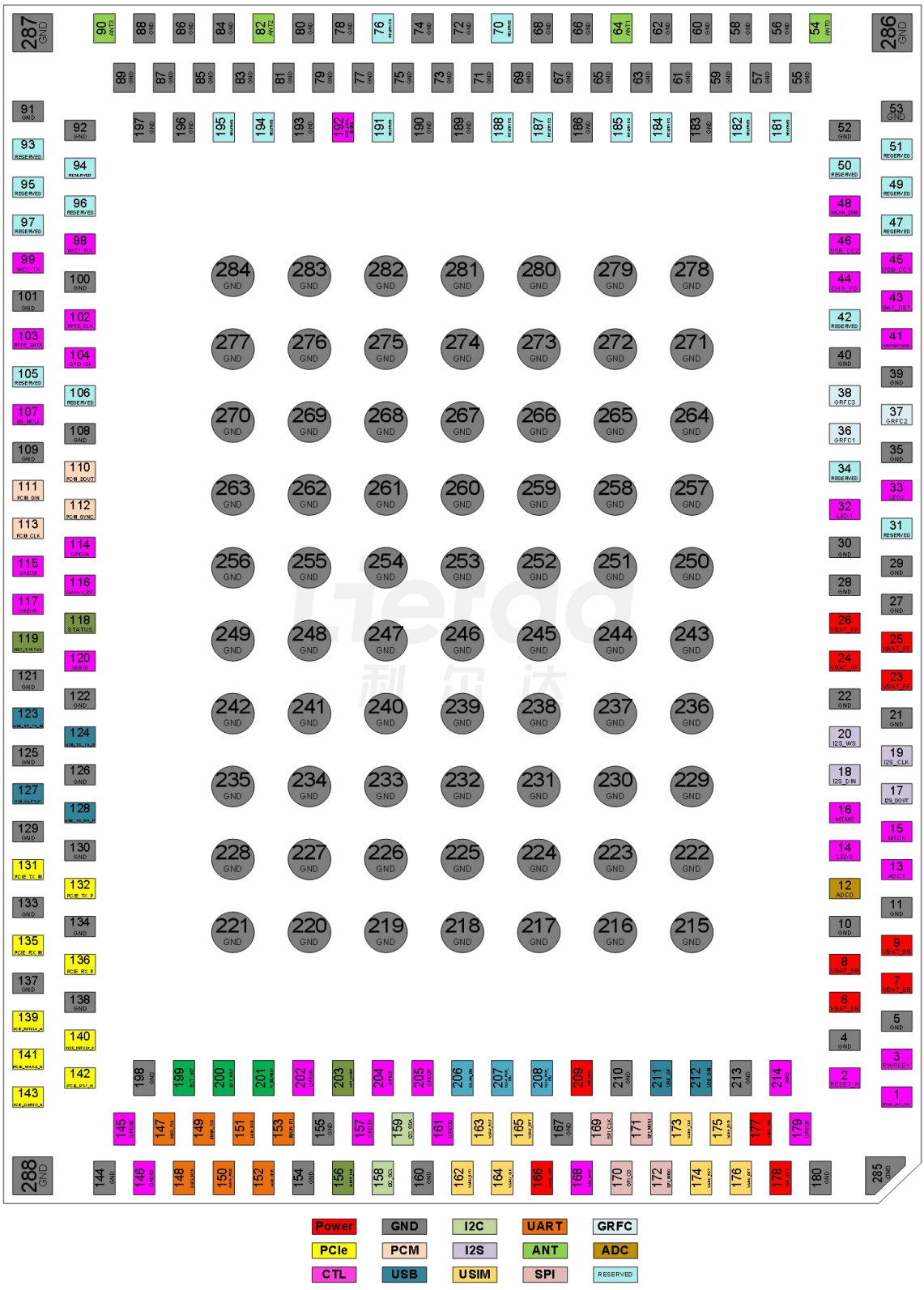


Figure 2.2 Module Pinout Diagram

2.5 Pin Description Table

Table 2-3 I/O Type Definitions

Type	Description
PI	Power input signal
PO	Power output signal
DI	Digital input signal
DO	Digital output signal
AI	Simulated input signal
AO	Simulated output signal
DIO	Digital bidirectional input/output signal
OD	Leakage leads the way
VIL	Low-level input voltage
VIH	High-level input voltage
VOL	Low-level output voltage
VOH	High-level output voltage

Table 2-4 Pin Definitions

Pin names	Pin number	Note
GND	4, 5, 10,11,21, 22, 27~30, 35, 39, 40, 52, 53, 55~63, 65~69, 71~75, 77~81,83~89, 91, 92, 100, 101, 108, 109, 121, 122, 125, 126, 129, 130, 133, 134,137, 138, 144, 154, 155, 160, 167, 180, 183, 186, 189, 190, 193, 196~198, 210, 213, 215~288	Keep grounded.
RESERVED	31、34、42、47、49、50、51、70、76、93~97、105、106、181、182、184、185、187、188、191、194、195	Keep suspended.

Table 2-5 Pin Definitions

Foot number	Pin names	Type	Description	Note
1	WLAN_SLP_CLK	AO	WLAN sleep clock	External WLAN 32KHz clock
2	RESET_N	DI	Module reset	Low-level pulse valid.
3	PWRKEY	DI	Module power on/off.	Low level/low level pulse valid.
6	VBAT_BB	PI	Baseband power supply	The power supply must be able to provide a current of up to 3.0A.
7	VBAT_BB			
8	VBAT_BB			
9	VBAT_BB			
12	ADC0	AI	General ADC interface	Voltage range: 0 ~ VBAT;
13	ADC1	AI	Universal ADC interface	Voltage range: 0 ~ VBAT;
14	LED0	AI	LED input 0	Maximum sink current 20mA
15	MTCK	DI	JTAG test clock input	JTAG test clock input
16	MTMS	DI	Selecting JTAG test mode	Selecting JTAG test mode
17	I2S_DOUT	DO	I2S data output	1.8V power domain; If not used, leave floating.
18	I2S_DIN	DI	I2S data input	1.8V power domain; If not used, leave floating.
19	I2S_CLK	DO	I2S clock	1.8V power domain; If not used, leave floating.
20	I2S_WS	DO	I2S field selection	1.8V power domain; If not used, leave floating.
23	VBAT_RF	PI	RF power module	The power supply must be able to provide a current of up to 3.0A.
24	VBAT_RF			
25	VBAT_RF			
26	VBAT_RF			
32	LED1	AI	LED input 1	The maximum sink current is 20mA.
33	LED2	AI	LED input 2	Maximum sink current 20mA
36	GRFC1	DO	Universal	1.8V power domain; compatible

Foot number	Pin names	Type	Description	Note
			Radio Frequency Control	with Bcode function.
37	GRFC2	DO	Universal Radio Frequency Control	1.8V power domain; If not used, leave floating.
38	GRFC3	DO	Universal Radio Frequency Control	1.8V power domain; If not used, leave floating.
41	VDD_SDCORE	PO	SD card power	Default closed, customization software needed to open
43	BAT_DET	AI	Battery in place detection	Battery in place detection; no need to connect to GND.
44	CHG_PD	DO	External charging enable control	Enable control pin for external charging IC
45	USB_CC1	AIO	Charging CC identification control 1	Check the pins.
46	USB_CC2	AIO	Charging CC Identification Control 2	Check the pins
48	WLAN_26M	AO	26MHz WLAN clock	External WLAN 26MHz clock
54	ANT0	AIO	Antenna 0 Interface	
64	ANT1	AIO	Antenna 1 interface	
82	ANT2	AIO	Antenna 2 interface	
90	ANT3	AIO	Antenna 3 Interface	
98	WCI_RX	DI	NR/WLAN coexistence reception	1.8V power domain; If not used, leave floating.

Foot number	Pin names	Type	Description	Note
99	WCI_TX	DO	NR/WLAN coexistence transmission	1.8V power domain; If not used, leave floating.
102	RFFE_CLK	DO	MIPI RFFE clock	1.8V power domain; If not used, leave floating.
103	RFFE_DATA	DIO	MIPI RFFE data	1.8V power domain; If not used, leave floating.
104	GPIO154	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
107	I2S_MCLK	DO	I2S master clock output signal	1.8V power domain; If not used, leave floating.
110	PCM_DOUT	DO	PCM data output	1.8V power domain; If not used, leave floating.
111	PCM_DIN	DI	PCM data input	1.8V power domain; If not used, leave floating.
112	PCM_SYNC	DO	PCM frame synchronization	1.8V power domain; If not used, leave floating.
113	PCM_CLK	DO	PCM clock	1.8V power domain; If not used, leave floating.
114	GPIO94	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
115	GPIO19	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
116	Factory_RST	DI	Restore to factory settings	1.8V power domain; If not used, leave floating.
117	GPIO18	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
118	STATUS	DO	Running status indicator	1.8V power domain; If not used, leave floating.
119	NET_STATUS	DO	Network status indicator	1.8V power domain; If not used, leave floating.
120	USB ID	DI	USB 2.0 OTG device detected.	1.8V power domain, leave floating if not used.
123	USB_SS_TX_M	AO	USB 3.0 transmission (-)	Compliant with USB 3.0 specifications; requires 90 Ω

Foot number	Pin names	Type	Description	Note
124	USB_SS_TX_P	AO	USB 3.0 transmission (+)	differential impedance. If not used, leave floating.
127	USB_SS_RX_M	AI	USB 3.0 receiving (-)	Compliant with USB 3.0 specification; Requires 90 Ω differential impedance. If not used, leave floating.
128	USB_SS_RX_P	AI	USB 3.0 reception(+)	
131	PCIE_TX_M	AO	PCIe transmission (-)	Support PCIe Gen2; Differential impedance requirement is 100 Ω
132	PCIE_TX_P	AO	PCIe transmission (+)	
135	PCIE_RX_M	AI	PCIe receive (-)	Support PCIe Gen2; Differential impedance requirement is 100 Ω
136	PCIE_RX_P	AI	PCIe receive (+)	
139	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	Supports PCIe Gen2; Differential impedance requirement of 100 Ω
140	PCIE_REFCLK_P	AIO	PCIe reference clock (+)	
141	PCIE_WAKE_N	DIO	PCIe wake-up	1.8V power domain; as master (slave) mode, this pin is for input (output) signal.
142	PCIE_RST_N	DIO	PCIe reset	1.8V power domain; as master (slave) mode, this pin is output (input) signal.
143	PCIE_CLKREQ	DIO	PCIe clock request	1.8V power domain; In master (slave) mode, this pin is for input (output) signal.
145	GPIO90	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
146	GPIO89	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
147	DBG_TXD	DO	Debugging serial port transmission	1.8V power domain, leave floating if not used.
148	DBG_RXD	DI	Debugging serial port	1.8V power domain, leave floating if not used.

Foot number	Pin names	Type	Description	Note
			reception	
149	MAIN_TXD	DO	Main serial port transmission	1.8V power domain, leave floating if not used.
150	MAIN_RXD	DI	Main serial port receiving	1.8V power domain, leave floating if not used.
151	MAIN_DCD	DO	Master serial port output carrier detection	1.8V power domain, leave floating if not used.
152	MAIN_DTR	DI	Main serial port data terminal ready/sleep wake-up	1.8V power domain, leave floating if not used.
153	MAIN_RI	DO	Main serial port outputs ringing prompt.	1.8V power domain, leave floating if not used.
156	SLEEP_IND	DO	Sleep status indicator	1.8V power domain; If not used, leave floating.
157	GPIO33	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
158	I2C_SCL	OD	I2C serial clock	1.8V power domain; If not used, leave floating. Requires external 1.8 V pull-up;
159	I2C_SDA	OD	I2C serial data	1.8V power domain; If not used, leave floating. Requires an external 1.8 V pull-up;
161	GPIO32	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
162	USIM2_DATA	DIO	SIM2 card data	USIM2_VDD1.8/3.0 V; If not used, leave floating.
163	USIM2_RST	DO	(U)SIM2 card reset	USIM2_VDD1.8/3.0 V; If not used, leave floating.
164	USIM2_CLK	DO	(U)SIM2 card clock	USIM2_VDD1.8/3.0 V; If not used, leave floating.
165	USIM2_DET	DI	SIM2 card detection	1.8V power domain; If not used, leave floating.

Foot number	Pin names	Type	Description	Note
166	USIM2_VDD	PO	(U)SIM2 power supply	The module automatically recognizes 1.8V or 3.0V USIM card.
168	USB_BOOT	DI	Forced download mode control. High level effective.	1.8V power domain; Suggest reserving test points.
169	SPI_CLK	DO	SPI Clock	1.8V power domain.
170	SPI_CS	DO	SPI chip select	1.8V power domain.
171	SPI_MOSI	DO	SPI master output from input	1.8V power domain, SPI only supports master mode.
172	SPI_MISO	DI	SPI main input from output	1.8V power domain; SPI only supports master mode.
173	USIM1_CLK	DO	SIM1 card clock	USIM1_VDD1.8/3.0 V; If not used, leave floating.
174	USIM1_RST	DO	SIM1 card reset	USIM1_VDD1.8/3.0 V; If not used, leave floating.
175	USIM1_DATA	DIO	SIM1 card data	USIM1_VDD1.8/3.0 V; If not used, leave floating.
176	USIM1_DET	DI	SIM1 card detection	1.8V power domain; If not used, leave floating.
177	USIM1_VDD	PO	SIM1 card power supply	The module automatically recognizes 1.8V or 3.0V
178	VDD_EXT	PO	External circuit powered at 1.8V	Can be used for external pull-up, maximum output 50mA; If not used, leave floating.
179	GPIO26	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
192	N79_LNA_disable	DO	WIFI coexistence control signal	If not used, leave floating.
199	EXT_INT	DI	External audio interruption	1.8V power domain.
200	EXT_RST	DO	External audio reset	1.8V power domain.

Foot number	Pin names	Type	Description	Note
201	W_DISABLE#	DI	Flight mode control	1.8V power domain.
202	GPIO95	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
203	NET_MODE	DO	Network registration indication	1.8V power domain; If not used, leave floating.
204	GPIO8	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
205	GPIO28	DO	Normal GPIO configuration	1.8V power domain; If not used, leave floating.
206	WLAN_EN	DO	WLAN enabled	1.8V power domain.
207	WLAN_PWR_EN1	DO	Control WLAN PA power supply.	1.8V power domain.
208	WLAN_PWR_EN2	DO	Control WLAN other power	1.8V power domain.
209	USB_VBUS	PI	USB detection	Vmax = 5.25 V Vnom = 5.0 V Vmin = 3.4 V
211	USB_DP	AIO	USB differential data (+)	Compliant with USB 2.0 specifications; impedance 90Ω.
212	USB_DM	AIO	USB differential data (-)	
214	WPS	DI	WPS function	1.8V power domain; If not used, leave floating.

2.6 Evaluation suite

Lierda can provide a complete evaluation and development kit, including an ADP board for easy debugging of the minimum system, an EVB board containing peripherals such as audio, RS485, SLIC, WIFI, and other accessories for development convenience.

3 Working Characteristics

3.1 Explanation of working mode

Table 3-1 Module Operating Modes Description

Working mode	Function	
Normal working mode	IDLE	The software is running normally. The module is registered on the network and can receive and send data.
	Talk/Data	The network connection is working properly. In this mode, the module's power consumption depends on the network settings and data transmission rate.
Minimum Function Mode	In the case of no power supply, using AT+CFUN=0 can set the module to the minimum functionality mode. In this mode, the RF does not work.	
Airplane mode	AT+CFUN=4 or lowering the W_DISABLE# pin can set the module to flight mode. In this mode, the RF does not work.	
Sleep mode	In this mode, the module's power consumption will be reduced to a very low level, but the module can still receive paging, SMS, calls, and TCP/UDP data.	
Shutdown mode	In this mode, the PMU stops supplying power to the baseband and RF sections, the software stops working, and the serial port is not accessible.	

3.2 Hibernate/Sleep Mode

In sleep mode, the DRX function of the module can reduce the power consumption of the module and broadcast the DRX index cycle value through the wireless network. The following figure shows the relationship between DRX operating time and the current consumption in sleep mode of the module. The longer the DRX sleep cycle, the lower the power consumption.

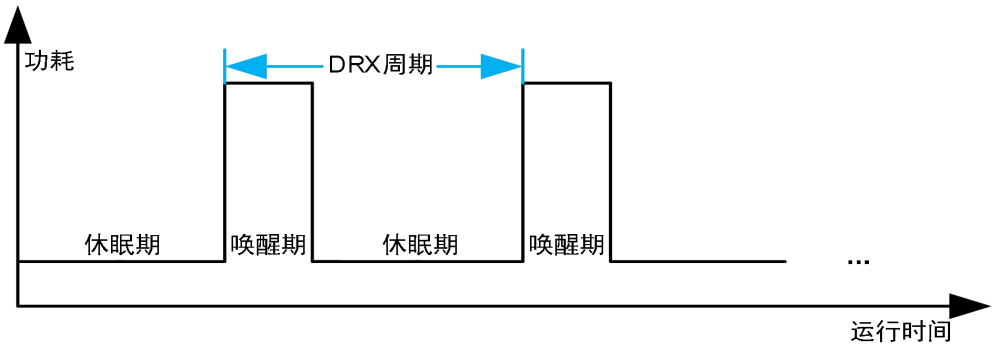


Figure 3.1 Relationship between DRX operation time and power consumption in sleep mode.

There are two scenarios for the NE26U-CN module to enter and exit sleep mode:

3.2.1 Serial port application scenarios

When the module is connected to the host computer via serial port, you can enter sleep mode by following these steps:

- Enable sleep function via the AT+LSCLK=1 command.
- Pull up MAIN_DTR.

The awakening steps are as follows:

- The host computer pulls down MAIN_DTR and keeps it low.

3.2.2 USB application scenarios

When the module is connected to the host computer via USB, you can enter sleep mode by following these steps:

- Enable sleep function via the AT+LSCLK=1 command.
- Pull up MAIN_DTR or float
- Port powered by USB_VBUS

The awakening steps are as follows:

- Inserting USB_VBUS will wake up the module.

3.3 Flight mode

The NE26U-CN module can control the flight mode on or off through the W_DISABLE# pin, and can also turn on or off the flight mode through AT commands. When the module

enters flight mode, the RF function cannot be used, and all AT commands related to RF cannot be accessed. Detailed description is as follows:

Table 3-2 Module supports two ways to enter flight mode

Serial number	Control mode	Control operation
1	Hardware I/O interface Key control	Pull up or suspend (default to pull up) W_DISABLE# for normal mode, pull down for flight mode.
2	AT command control	AT+CFUN=4--Enter flight mode AT+CFUN=0--Minimum functionality mode (turn off RF and SIM card) AT+CFUN=1--Full functionality mode

Hardware method:

W_DISABLE# pin is pulled up by default. Pulling down this pin will enable the flight mode of the module.

Table 3-3 W_DISABLE# Pin Description

Pin number	Pin name	Type	Description	Parameters	Note
201	W_DISABLE#	DI	Module flight mode control	1.8V voltage domain	If not used, leave float

The reference design of the W_DISABLE# interface is as shown in the following figure.

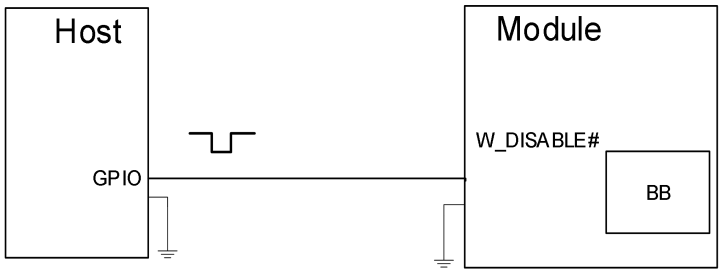


Figure 3.2 W_DISABLE# Interface Reference Circuit

3.4 Power supply design

3.4.1 Power interface

The module has 8 VBAT pins for connecting external power, which can be divided into two voltage domains:

4 VBAT_RF pins are used to supply RF power to the module.

4 VBAT_BB pins are used to supply power to the baseband of the module.

In addition, the module reserves 2 external power supply routes. VDD_EXT is open by default for direct use, while VDD_SDCORE is closed by default and needs customized software to be opened for use.

Table 3-4 Power Supply Pin Definitions

Pin number	Type	Pin names	Description	Minimum value	Typical value	Maximum value	Unit
6,7,8,9	PI	VBAT_BB	Baseband section power supply	3.3	3.8	4.3	V
23,24,25,26	PI	VBAT_RF	RF section power supply	3.3	3.8	4.3	V
178	PO	VDD_EXT	External 1.8V power supply Maximum output 50mA	-	1.85	-	V
41	PO	VDD_SDCORE*	SD card power Default closed	1.8	*	3.3	V

Note

*Indicates that the interface function is under development and not yet supported. If you need to use it, please contact our FAE for confirmation.

3.4.2 Power supply design requirements

To ensure the normal operation of the NE26U-CN module, the system power supply VBAT needs to be maintained within the range of 3.3V-4.3V (typical value 3.8V). When the module is used with different external devices, attention should be paid to the power supply

design of the module. In any case, it is necessary to ensure that the module power supply voltage remains above 3.3V, otherwise the module will not function properly, and it is also recommended that the Ripple be less than 0.1V.

The power supply requires a waveform as shown in the following figure:

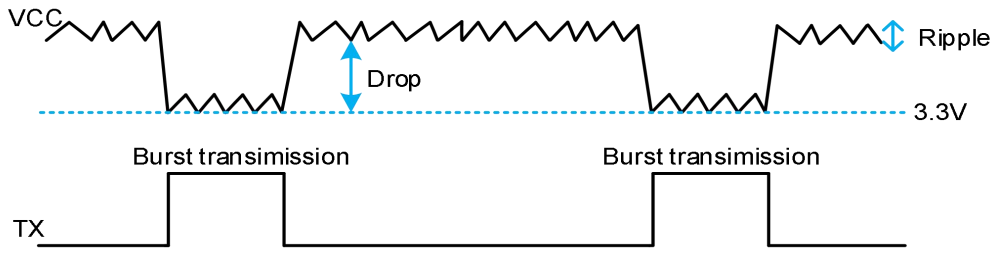


Figure 3.3 Power Requirements During Operation

External power supply LDO or DCDC selection recommendations for devices capable of providing a current of 3A or above. Additionally, to minimize the impact of PCB traces on power supply, VBAT_BB and VBAT_RF should adopt a star wiring pattern, with VBAT_BB trace width not less than 2mm, and VBAT_RF trace width not less than 2.5mm. In principle, the longer the VBAT trace, the wider the trace width.

3.4.3 Recommend design and reference circuit.

To reduce voltage drops, it is necessary to parallel at least one 220uF energy storage capacitor on VBAT_BB and VBAT_RF respectively, and reserve three ceramic capacitors for VBAT_BB and VBAT_RF separately, with the capacitors placed close to the power supply pins. In addition, to improve the stability of the power supply, it is recommended to add a TVS diode near VBAT.

Table 3-5 Capacitor Description

Recommend capacitors.	Application	Explanation
220uF×2	Stabilizing tantalum capacitor	Reduce the power supply fluctuation during the operation of the module, and request the use of low ESR (ESR=0.7Ω) capacitors.

		(1) The power supply requirement for LDO or DCDC should not be less than 440uF capacitance. (2) The battery power supply can be appropriately reduced to 100-220uF capacitance.
1uF，100nF	Digital signal noise	Filter out interference generated by clocks and digital signals.
33pF	700, 850/900MHz frequency band	Remove low-frequency RF interference.
8.2pF	1700/1800/1900, 2100/2300, 2500/2600MHz frequency bands	Filter out RF interference in the mid/high frequency bands.

The reference circuit is shown in the following figure.

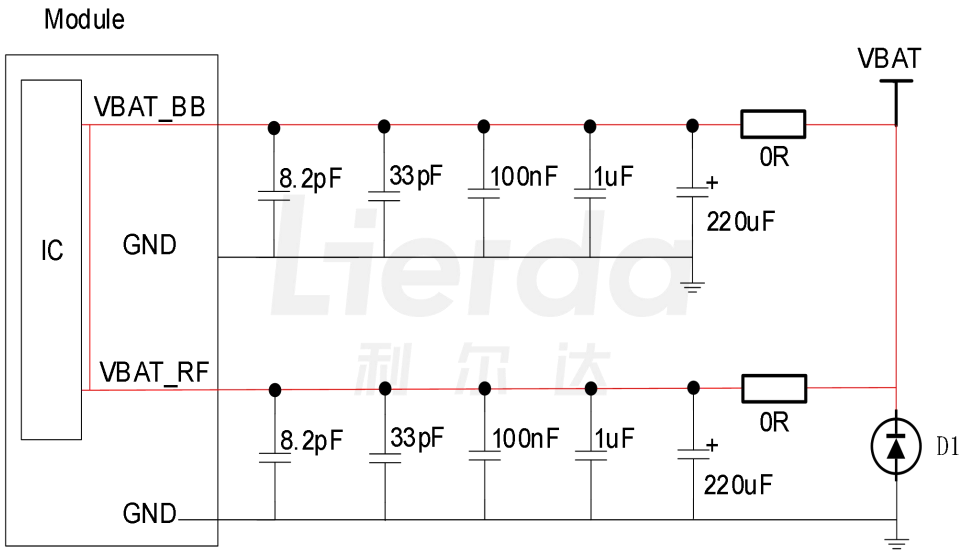


Figure 3.4 Power Supply Recommendation Design

3.5 Power on/off

The NE26U-CN module implements power on and off through the PWRKEY pin.

Table 3-6 PWRKEY Interface Description

Pin numbe	Pin names	Type	Describe	Para meter	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
3	PWRKEY	DI	Module power on/off	VIH	1.5	-	VBAT	Low level/low level pulse is valid. The

Pin numbe	Pin names	Type	Describe	Para meter	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
				VIL	-	-	0.2	

3.5.1 Power on.

When the NE26U-CN module is in power-on shutdown mode, the module can be powered on by pulling down PWRKEY for at least 1.2 seconds, which can be done using a GPIO signal or a button.

- The host powers on by pulling down the PWRKEY pin through GPIO, the reference circuit is as shown below.

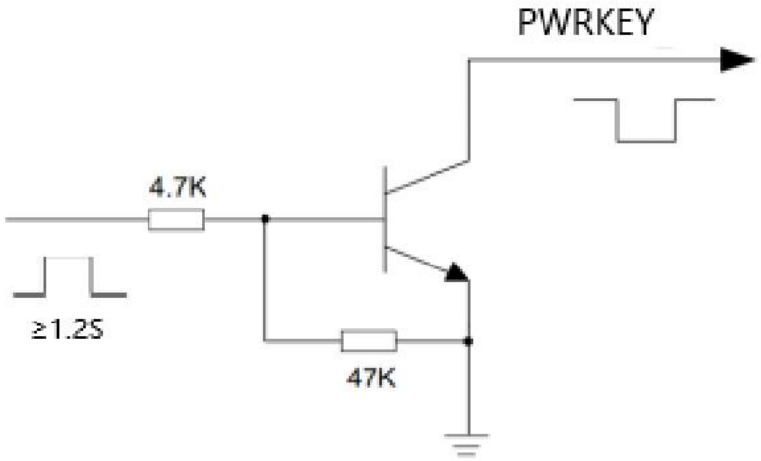


Figure 3.5 GPIO module boot control

- By connecting the PWRKEY pin, the power can be turned on. A TVS is reserved for ESD protection. Please refer to the circuit diagram below.

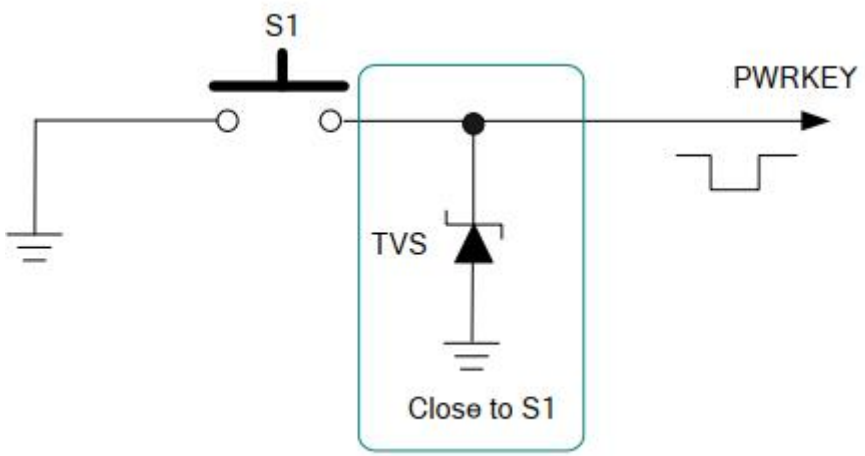


Figure 3.6 Power on by pressing the button

The power-on sequence is as shown in the following figure.

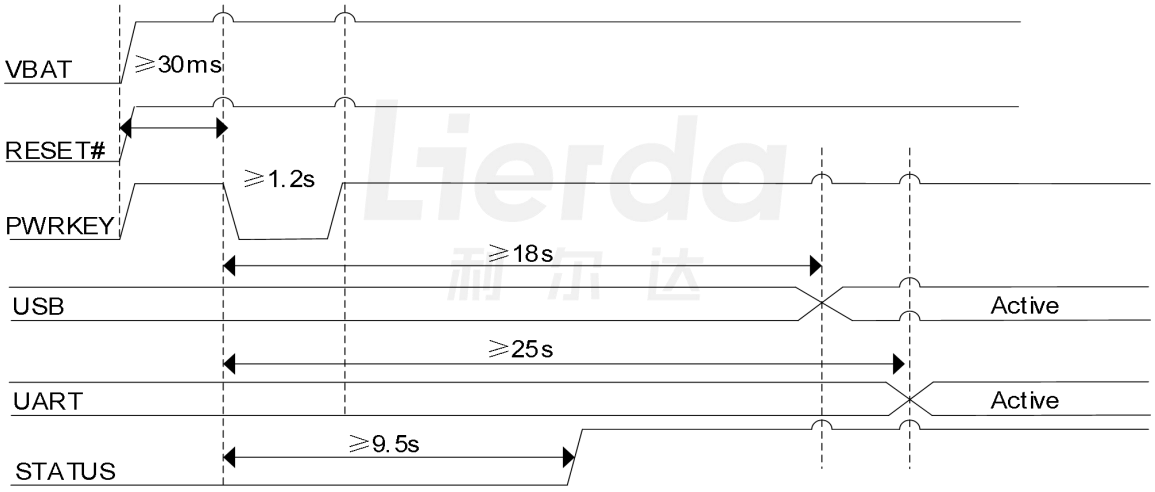


Figure 3.7 Power-on Timing Diagram

Note

Before pulling up the PWRKEY pin, ensure that the VBAT voltage is stable. It is recommended that the time interval between powering up VBAT and pulling up the PWRKEY pin should not be less than 30 ms. The timing here is related to the operations of UART and USB during startup. In terms of the time for AT commands, the difference between the two timings is not significant.

3.5.2 Shutdown

When the module is in the power-on state, the host pulls down the PWRKEY pin, and the module will execute the shutdown process, which takes about 3 seconds.

In addition, the shutdown can also be done through the AT+LPOWD command. The command has the same function as pulling down PWRKEY to shut down.

Shutdown timing sequence is shown in the figure below:

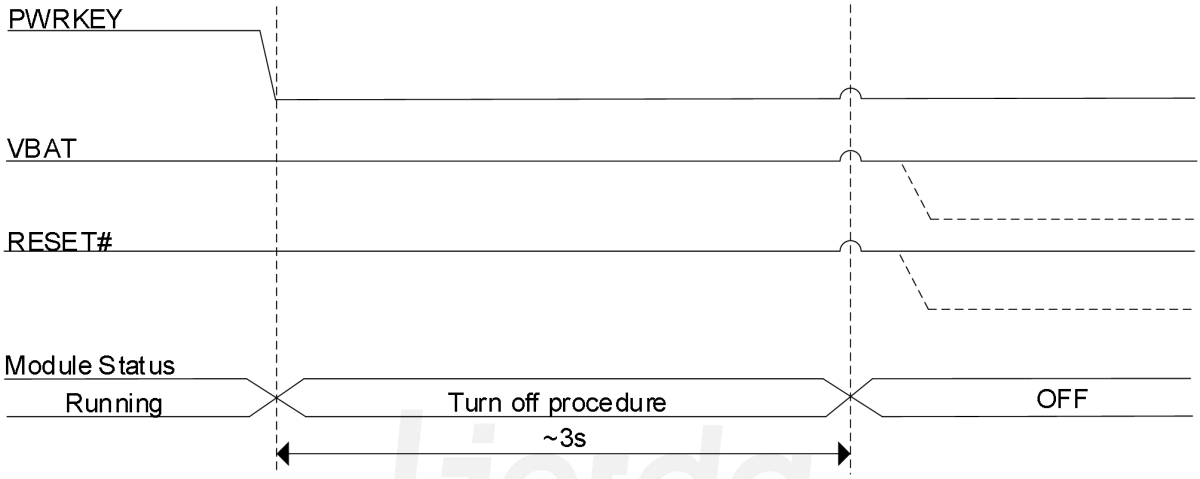


Figure 3.8 Shutdown Timing Diagram

Note

When the module is working normally, do not cut off the power supply immediately to avoid damaging the Flash inside the module. It is recommended to first turn off the module through PWRKEY or AT+LPOWD, and then cut off the power supply.

After the AT command is executed successfully, it will return OK. Then the UE activates the network and enters the power down state by outputting POWER DOWN. The maximum duration for network activation is 60 seconds, so the customer needs to pay attention to the shutdown time in the design. To avoid data loss, the module must not be powered off before outputting POWER DOWN.

3.6 Reset

The NE26U-CN module can be reset by using the RESET# pin.

Table 3-7 RESET_N Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
2	RESET_N	DI	Module reset	VIH	1.5	-	VBAT	Low-level pulse is effective. Internally pulled up to VBAT through 20K.
				VIL	0	-	0.5	

After the module is powered on, pulling down the RESET_N pin for 250ms or longer can reset the module. The RESET# signal is sensitive to interference, so it is recommended to keep the traces on the module interface board as short as possible and include GND handling.

Customers can use an open-drain drive circuit or a button to control the RESET# pin, refer to the circuit as shown in the diagram below.

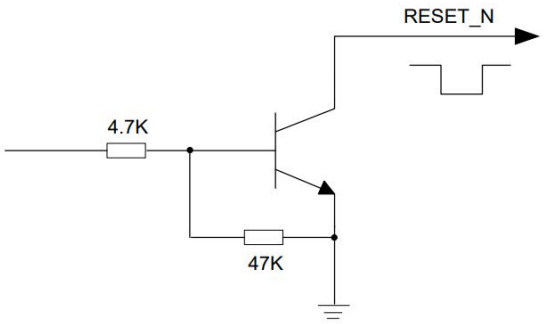


Figure 3.9 Open-Drain Driven Reset Reference Circuit

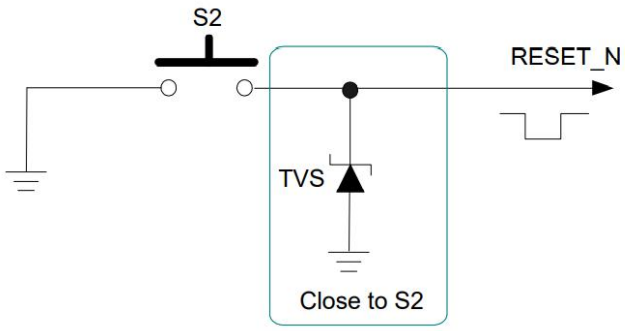


Figure 3.10 Key Reset Reference Circuit

The reset timing diagram is as follows:

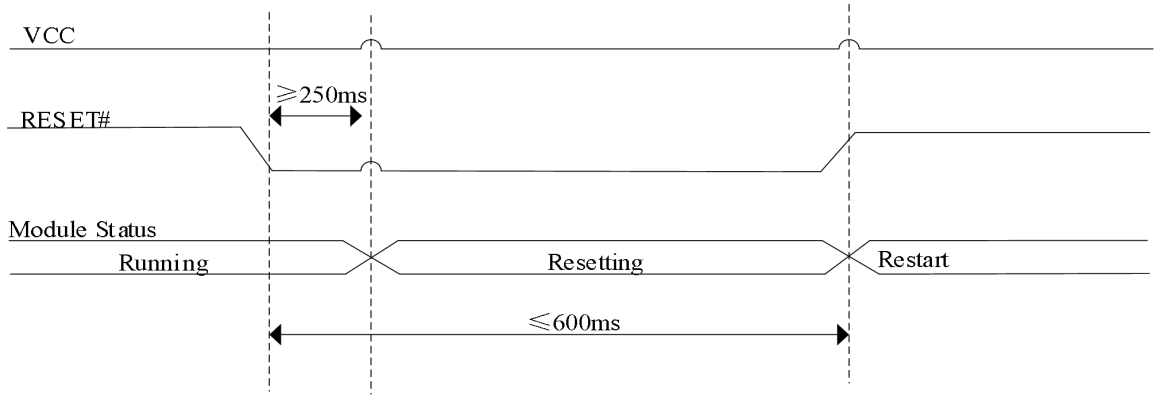


Figure 3.11 RESET# Timing Diagram

Note

- Ensure that the maximum load capacitance for the PWRKEY and RESET_N pins does not exceed 47pF.
- The reset function is recommended to be used only after the AT+LPOWD command and PWRKEY shutdown fail.

4 Application Interface

This chapter mainly introduces the definition and related applications of the NE26U-CN interface.

- UART interface
- USB interface
- PCIe interface
- (U)SIM interface
- I2C interface
- PCM/I2S and SPI interfaces
- ADC interface
- Status indicator interface
- USB_BOOT interface
- WIFI control interface
- Antenna tuning control interface*
- B code time synchronization interface*
- LED interface *
- Charging expansion interface*
- GPIO interface
- Other function interfaces
- Antenna interface

4.1 UART interface

The NE26U-CN module has 2 serial ports: the main serial port and the debug serial port. The main features are as follows:

- The main serial port can be used for AT command sending and data transmission, with a default baud rate of 115200bps.
- Debug the serial port for partial log printing, with a default baud rate of 115200bps.

Table 4-1 Main Serial Port Interface Pin Description

Pin number	Pin name	Type	Description	Parameters	Minimum value (V)	Typical Value (V)	Maximum value (V)	Note
149	MAIN_TXD	DO	Main serial port transmission	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
150	MAIN_RXD	DI	Main serial port reception	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
151	MAIN_DCD	DO	Main serial port carrier detection	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
152	MAIN_DTR	DI	The main serial port receives data. Wake/Sleep Activation	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
153	MAIN_RI	DO	Main serial port ringing prompt	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	

Table 4-2 Debug Serial Port Interface Pin Description

Pin numb	Pin name	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
148	DBG_RXD	DI	Debugging serial port reception	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
147	DBG_TXD	DO	Debug serial port transmission	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	

When using the serial port, pay attention to the issue of level consistency. The module's serial port level is 1.8V. If you need to connect to different levels such as 3.3V, you need to add a level conversion circuit. Details are as follows:

4.1.1 Transistor level shifting reference circuit

This circuit does not have special requirements for the power supply voltage of the module, and it is low cost, but there are limitations on the serial port baud rate. The reference design is as follows, also pay attention to the direction of level conversion.

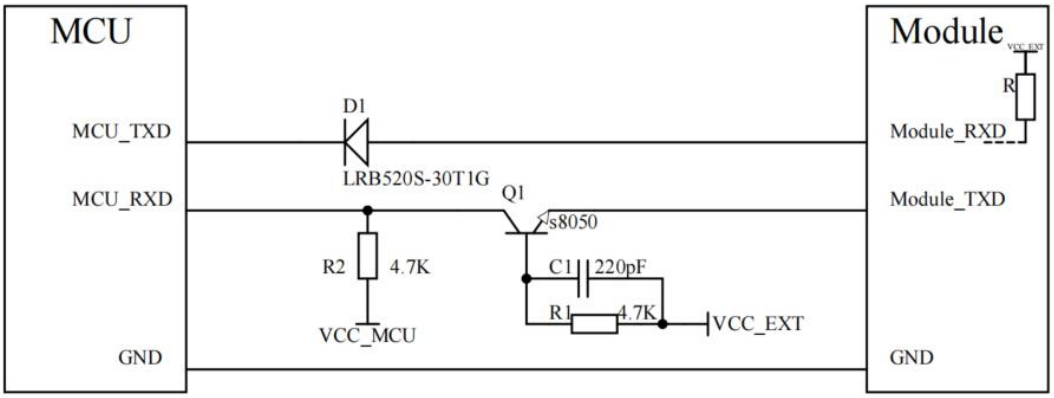


Figure 4.1 Transistor Level Conversion Reference Circuit

Note

- If the module does not have internal pull-up, the user of the diode conversion circuit needs to have an external pull-up. The NE26U-CN internally pulls up through a 20K resistor to a 1.8V voltage domain.
- In this circuit, MCU_TXD defaults to outputting 3.3V, and VDD_EXT (RFFE_VIO_1V8) defaults to 1.85V. For the diode conversion circuit, it should be noted that the cathode voltage of the diode needs to be higher than the anode voltage in order to achieve the function of the circuit mentioned above.
- This voltage conversion circuit is not suitable for applications with a baud rate exceeding 460Kbps.

4.1.2 MOSFET level conversion reference circuit

This circuit does not have special requirements for the power supply voltage of the module, and it is low cost, capable of meeting the requirement of serial port baud rate

921600bps. The reference design is as follows, pay attention to the direction of level conversion.

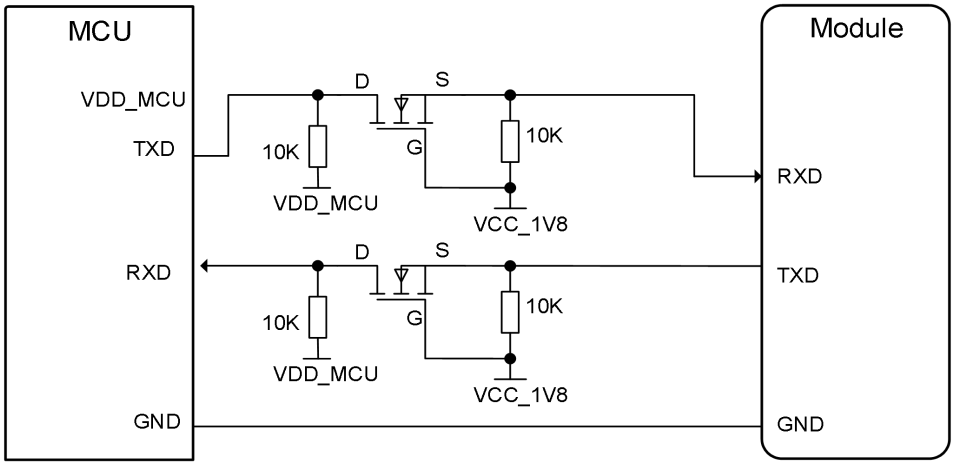


Figure 4.2 MOSFET level conversion reference circuit

Recommend MOSFET for reference:

Brand: LRC; Specification model: L2N7002LT1G, the corresponding internal principle is as follows:

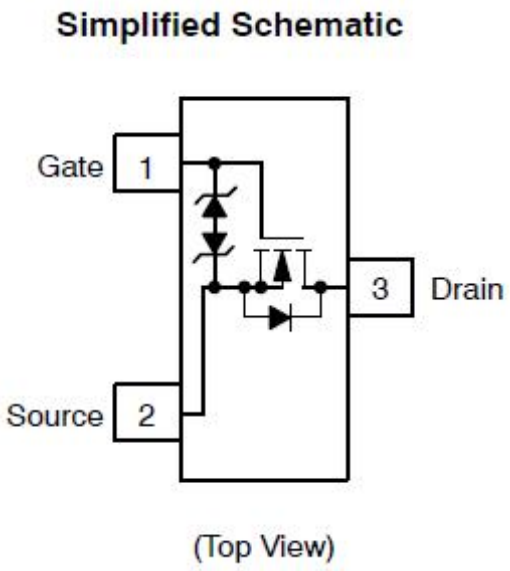


Figure 4.3 MOSFET device diagram

4.1.3 Reference circuit for level conversion chip

This circuit has a slightly higher cost, but a higher data rate, which can meet the typical usage requirements of serial ports. It is recommended to use the TXS0108EPWR from TI.

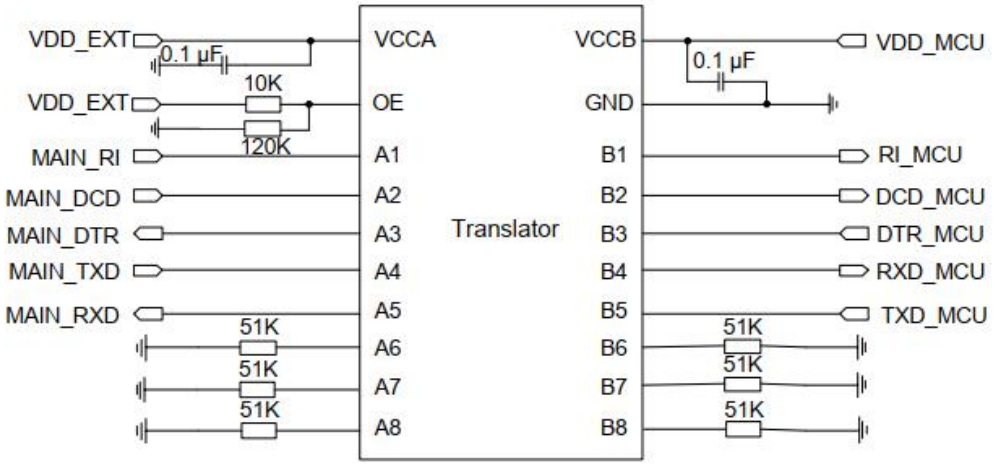


Figure 4.4 Level Shifting Chip Circuit

4.2 USB interface

The NE26U-CN module supports 1 USB interface, the interface complies with USB 2.0 and 3.0 specifications, and supports USB 2.0 high-speed (480Mbps) and full-speed (12Mbps) modes, as well as USB 3.0 super-speed (5Gbps) mode. The USB interface can be used for AT command transmission, data transfer, software debugging, and firmware upgrades. The table below shows the pin definitions for the USB interface.

Table 4-3 USB Interface Pin Description

Pin number	Pin names	Type	Description	Note
211	USB_DP	AIO	USB differential data (+)	90Ω differential impedance
212	USB_DM	AIO	USB differential data (-)	
123	USB_SS_TX_M	AO	USB3.0 transmission (-)	
124	USB_SS_TX_P	AO	USB3.0 transmission (+)	
127	USB_SS_RX_M	AI	USB3.0 receiving (-)	
128	USB_SS_RX_P	AI	USB3.0 receiving(+)	

209	USB_VBUS	PI	USB detection	For USB detection only, not for power supply.
120	USB ID*	DI	OTG detection	The OTG function is not turned on by default.

Note

*Indicates that the interface function is under development and is not currently supported. If you need to use it, please contact our FAE for confirmation.

When advising customers on design, it is recommended to reserve test points for USB 2.0 interface for firmware upgrades and debugging. The reference circuits for USB 2.0 and USB 3.0 are as follows:

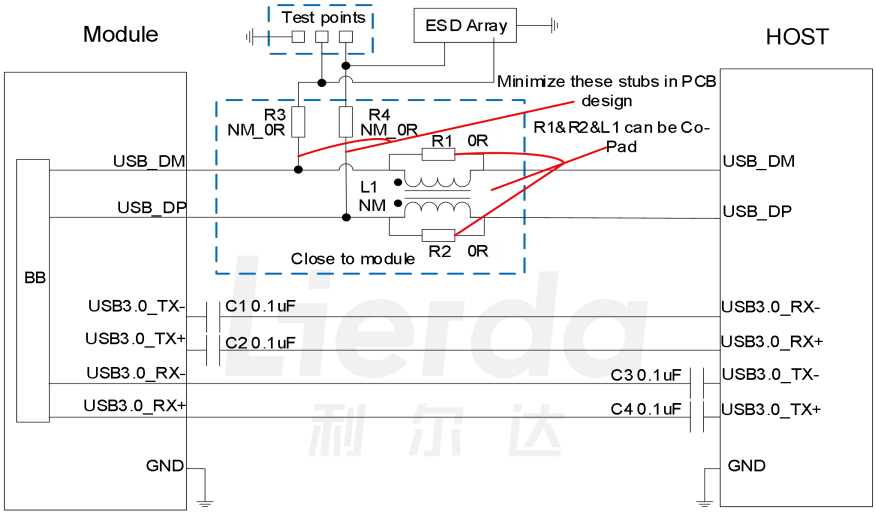


Figure 4.5 USB reference design diagram

Coupling capacitors C3 and C4 must be placed near the TX end of the host USB 3.0 interface, and the two capacitors must be positioned close to each other. Coupling capacitors C1 and C2 must be placed near the TX end of the module's USB 3.0 interface, and the two capacitors must be positioned close to each other.

Note:

- It is recommended to connect a common mode inductor L1 between the host and the module to prevent USB signal EMI interference. Alternatively, a 0Ω resistor can be used for direct connection, designed with a common pad with L1. Depending on the debugging situation, either a common mode inductor or a resistor can be used. Additionally, it is

suggested to connect resistors R3 and R4 to test points for debugging purposes, with the resistors not populated by default. To meet the USB data line signal integrity requirements, L1, R1, R2, R3, and R4 need to be placed close to the module, with R3 and R4 placed close together. The routing between the connected test points should be kept as short as possible.

- In the circuit design of the USB interface, to ensure the performance of USB, the following principles are recommended to be followed in the circuit design: Ground should be wrapped around the USB routing, using 90Ω differential impedance lines. Do not route USB lines under crystal oscillators, oscillators, magnetic devices, DC-DC power inductors, and RF signals. It is recommended to use inner layer differential lines, and surround them with ground on all sides. When selecting ESD protection devices for USB data lines, pay attention to ensure that the parasitic capacitance of USB 2.0 does not exceed 1pF, and for USB 3.0 does not exceed 0.5pF. Place the ESD protection device as close to the USB interface as possible, and ensure that the signal passes through the ESD protection device first.
- For USB3.0 signals, the differential pair routing should be kept as short as possible. When connecting type A/B connectors, the length should not exceed 100mm. When connecting microAB/micro B/type C connectors, the length should not exceed 220mm. For TXP/TXN and RXP/RXN differential pairs, the intra-pair line length difference should not exceed 0.15mm.

4.3 PCIe interface

The NE26U-CN module contains a PCIe interface that complies with the PCIe 2.0 specification. It supports EP and RC modes, and the PCIe operating mode can be configured through AT+LCFG="pcie/mode",1 (0 for EP, 1 for RC, restart required for changes to take effect). The default mode is RC, for more details on relevant AT commands, please refer to the "AT+LCFG="pcie/mode"" section in the NE26U_CN AT Command Manual. The main features of the PCIe interface are as follows:

- Support PCIe Gen2 (5Gbps max), backward compatible
- Support PCIe to Ethernet conversion.
- Support RC and EP modes.

Table 4-4 PCIe Interface Pin Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical Value (V)	Maximum value (V)	Note
131	PCIE_TX_M	AO	PCIe transmits data (-)					
132	PCIE_TX_P	AO	PCIe transmits data (+)					
135	PCIE_RX_M	AI	PCIe receive data (-)					
136	PCIE_RX_P	AI	PCIe receive data (+)					
139	PCIE_REFCLK_M	AIO	PCIe reference clock (-)					RC mode: output (default) EP Mode: Input
140	PCIE_REFCLK_P	AIO	PCIE reference clock (+)					
141	PCIE_WAKE_N	DIO	PCIe wake-up					RC mode: Input (default) EP Mode: Output
142	PCIE_RST_N	DIO	PCIe reset					RC mode: Output (default) EP Mode: Input
143	PCIE_CLKREQ_N	DIO	PCIe clock request					RC mode: Input (default) EP Mode: Output

NE26U-CN PCIe interface has slight hardware circuit differences when operating in RC mode and EP mode. The following diagram shows the reference circuit of NE26U-CN using PCIe interface to connect PCIe devices and hosts:

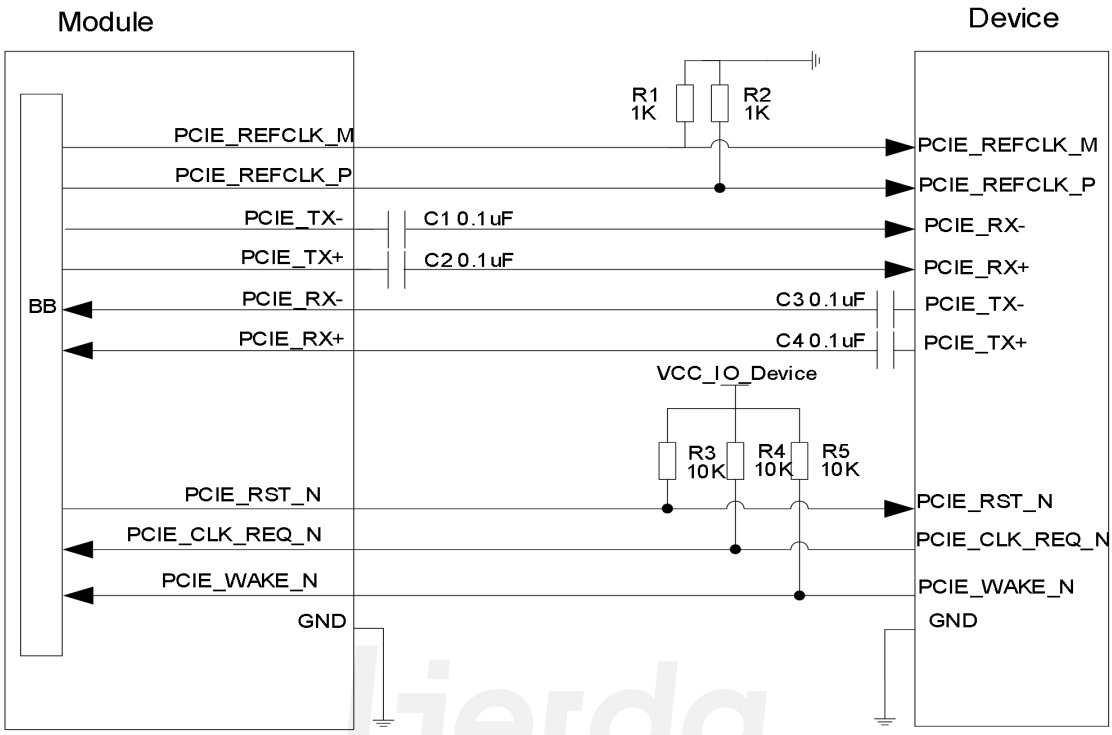


Figure 4.6 Reference Design Diagram for Module Connection to PCIe Devices (RC Mode)

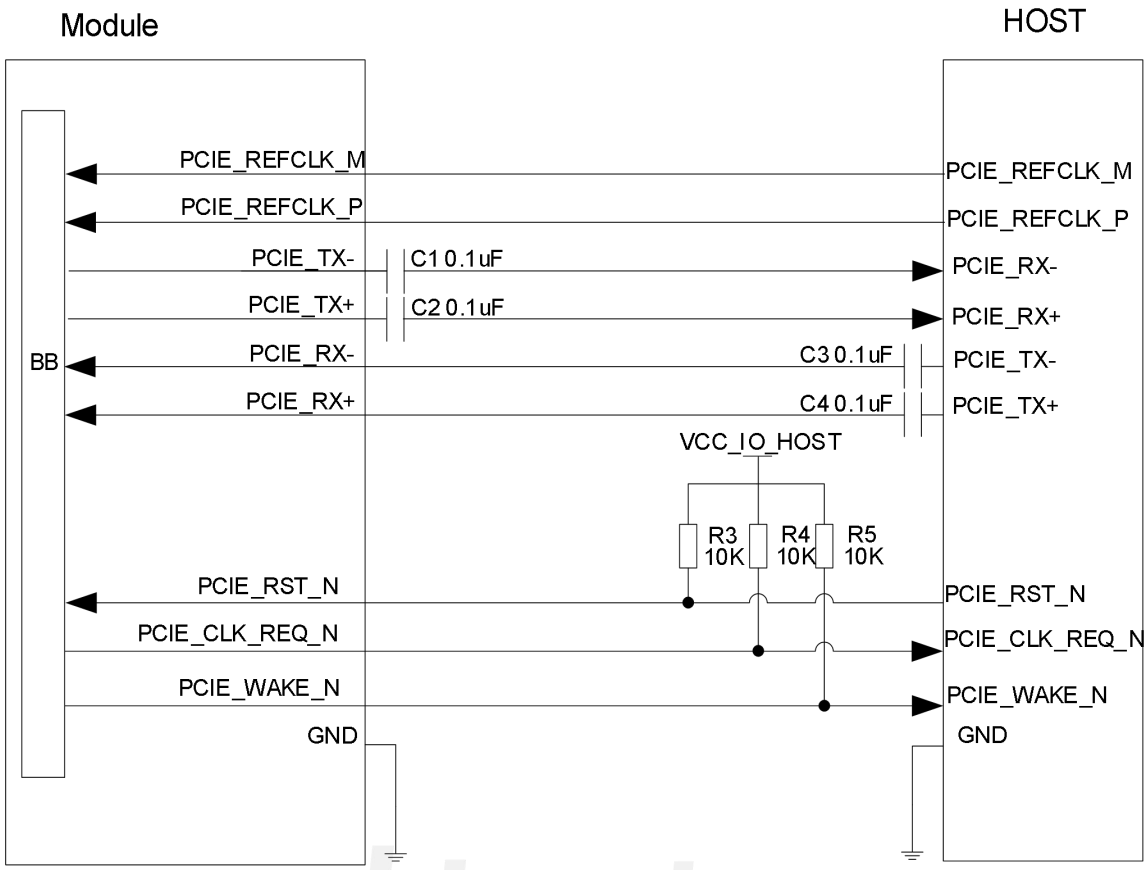


Figure 4.7 Reference Design for Module Connection to PCIe Host (EP Mode)

Note

- Capacitors C1, C2, C3, C4 should be placed close to Tx PIN respectively, recommended to use 0.1uF, +/-10%, X5R or X7R.
- R1 and R2 two terminal resistors are recommended to use 1K.
- CLK, TX, and RX differential signal lines need to be routed with a differential impedance of 100Ω +/-10% controlled.
- When routing PCIe, stay away from sensitive signal sources such as RF, audio, and crystal oscillators.
- PCIe routing should not be placed below components and must not cross paths with other signals.
- CLK, TX, and RX three pairs of differential signal lines should be routed as short as possible, ideally controlled within 350mm, and maintain a 3W line width between differential pairs and other signals.

- CLK, TX, and RX should be routed in a three-dimensional manner with top, bottom, left, right, and GND for differential signal lines.
- When connecting to a host or PC in the 3.3V voltage domain, make sure to use a voltage conversion chip to maintain level compatibility.

4.4 (U)SIM card interface

4.4.1 (U)SIM pin description

The module supports 2 (U)SIM card interfaces, and both support hot swapping. The interfaces comply with ETSI and IMT-2000 card specifications, support 1.8V and 3.0V (U)SIM cards, and support dual SIM dual standby function. The table below describes the interface definition of (U)SIM.

Table 4-5 (U)SIM Card Interface Definition

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
174	USIM1_RST	DO	Reset (U)SIM1 card	VOH	1.62/2.1	1.85/3.0	1.98/3.3	If not used, leave floating
				VOL	0	-	0.18/0.3	
173	USIM1_CLK	DO	SIM1 card clock	VOH	1.62/2.1	1.85/3.0	1.98/3.3	If not used, leave floating
				VOL	0	-	0.18/0.3	
175	USIM1_DATA	DIO	SIM1 card data	VIH	1.2/2.1	1.85/3.0	1.98/3.3	If not used, leave floating
				VIL	0	-	0.54/0.9	
				VOH	1.62/2.1	1.85/3.0	1.98/3.3	
				VOL	0	-	0.18/0.3	
177	USIM1_VDD	PO	SIM1 card power	-	1.62	1.85/3.0	3.3	If not used, leave floating
176	USIM1_DET	DI	Detection of SIM1 card	VIH	1.26	1.85	1.98	Pay attention to logic insertion, software and
				VIL	0	-	0.54	
165	USIM2_DET	DI	Detection of (U)SIM2 card	VIH	1.26	1.85	1.98	
				VIL	0	-	0.54	

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
								hardware design should be consistent.
162	USIM2_DATA	DIO	SIM2 card data	VIH	1.2/2.1	1.85/3.0	1.98/3.3	If not used, leave floating
				VIL	0	-	0.54/0.9	
				VOH	1.62/2.1	1.85/3.0	1.98/3.3	
				VOL	0	-	0.18/0.3	
164	USIM2_CLK	DO	SIM2 card clock	VOH	1.62/2.1	1.85/3.0	1.98/3.3	If not used, leave floating
				VOL	0	-	0.18/0.3	
163	USIM2_RST	DO	Reset (U)SIM2 card	VOH	1.62/2.1	1.85/3.0	1.98/3.3	If not used, leave floating
				VOL	0	-	0.18/0.3	
166	USIM2_VDD	PO	(U)SIM2 card power	-	1.62	1.85/3.0	3.3	If not used, leave floating

The schematic diagram of the (U)SIM interface circuit design is as follows:

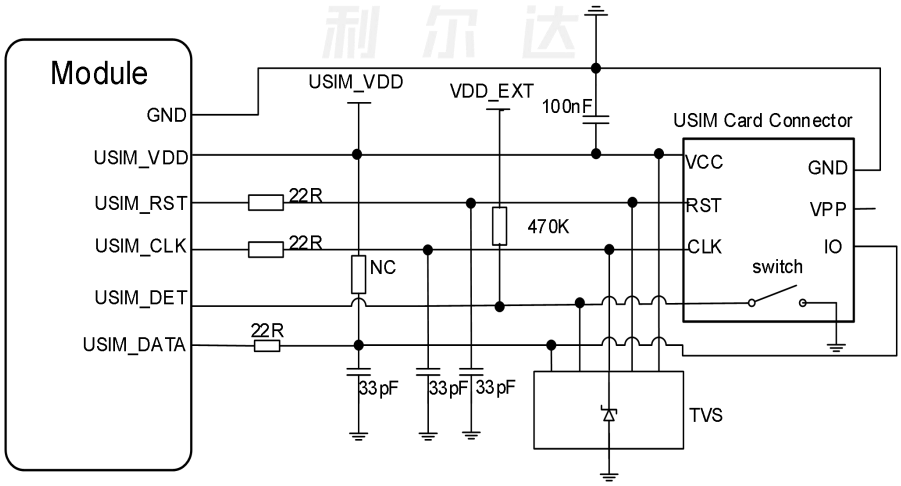


Figure 4.8 8-pin (U)SIM interface reference circuit diagram

The principle of the SIM card slot with detection signal is as follows (design should pay attention to the logic of card insertion). Taking the MUP-C792 card slot connector as an example, the specification sheet describes the Detect Switch as follows,

ELECTRIC FUNCTION	DETECT SWITCH
WITHOUT CARD	CLOSED
CARD INSERTED	OPEN

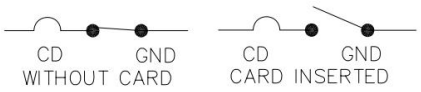


Figure 4.9 SIM card connector Detect Switch operation block diagram

When the SIM card is inserted, USIM_DET is high, and when the SIM card is removed, USIM_DET is low.

If the USIM card detection function is not needed, please leave the USIM_DET pin floating. The following is the 6-pin USIM interface reference circuit:

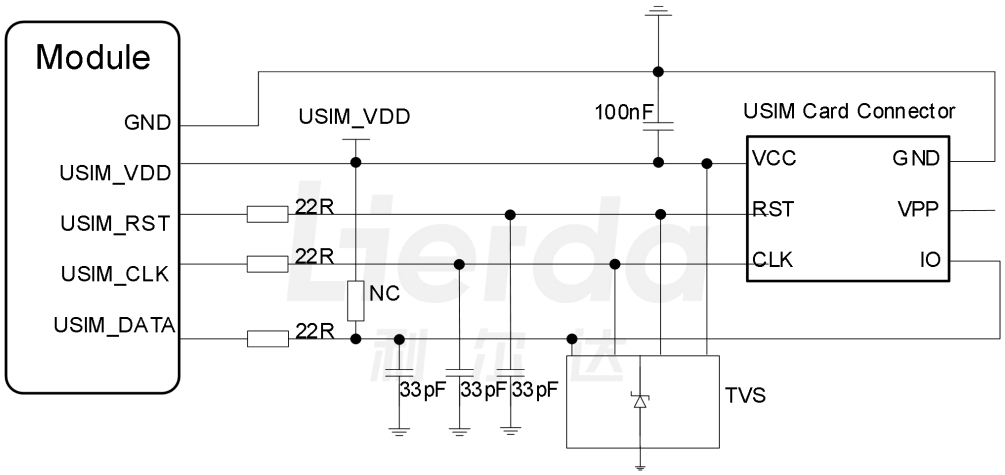


Figure 4.10 6-pin (U)SIM Interface Reference Circuit

4.4.2 (U)SIM hot swap

The NE26U-CN module supports (U)SIM card hot-swapping function, which determines the insertion and removal of (U)SIM cards by detecting the status of the USIM_DET pin of the (U)SIM card slot, thus supporting (U)SIM card hot-swapping function. The (U)SIM card hot-swapping function can be configured using the AT+LSIMDET command.

This command is used to query/enable/disable SIM card detection. GPIO interrupt is used to detect SIM card insertion, and the detection pin level needs to be set when

inserting the SIM card.

Test command: AT+LSIMDET=?	+LSIMDET:(Supported <enable> list),(Supported <insert_level> list)
Query command: AT+LSIMDET?	+LSIMDET:<enable>,<insert_level>
Command settings: AT+LSIMDET=<enable>,<insert_level>	<enable>. Enable/disable (U)SIM card detection function. 0: Disabled, 1: Enabled <insert_level>. Detect the level of the pins when inserting (U)SIM card. 0: Low level, 1: High level
Maximum response time	3 seconds
Feature Description	The command will take effect after restart; the parameter configuration will be automatically saved after configuration.

Table 4-6 USIM_DET Control Voltage Description

AT format	AT command	SIM card hot swap detection	Function Description
Read Command AT+LSIMSTAT? Write Command AT+LSIMSTAT=<enable>,<insert_level>	AT+LSIMDET=1,0	Start	(USIM) SIM card hot plug detection function enabled, the module detects whether the (U)SIM card is inserted by checking the state of the USIM_DET pin, low-level detection.
	AT+LSIMDET=1,1	Start	The (U)SIM card hot-plug detection function is enabled, and the module detects whether the (U)SIM card is inserted through the

			USIM_DET pin status detection, detecting a high level.
	AT+LSIMDET=0,0 AT+LSIMDET=0,1	Close	SIM card hot plug detection function is disabled, the module reads (U)SIM card during startup without checking USIM_DET status.

Note

- NE26U-CN module (U) SIM card hot swap function is enabled by default, and AT+LSIMDET=1,1.
- The <insert_level> value needs to match the insertion level of the hardware design, otherwise the hot swap function will be invalid.
- If a (U)SIM card has been successfully detected, the command to control the (U)SIM card detection function is no longer supported. The command to control the (U)SIM card detection function can only be used again after the module is restarted or the (U)SIM card is hot-swapped.

4.4.3 Requirements for (U)SIM card interface design

In the circuit design of the (U)SIM card interface, in order to ensure the good functional performance of the (U)SIM card and prevent damage, the following design principles are recommended to be followed in the circuit design:

- The distance between the (U)SIM card slot and the module bracket should not be too far, the closer the better, try to ensure that the (U)SIM card signal line wiring does not exceed 200mm.
- (U)SIM card signal line wiring should be kept away from RF lines and VBAT power lines.
- To prevent possible crosstalk from the USIM_CLK signal to the USIM_DATA signal, they should not be wired too close together. Ground shielding should be added between the

two traces, and ground protection is also needed for the USIM_RST signal.

- To ensure good ESD protection, it is recommended to add TVS diodes placed near the (U)SIM card holder. The parasitic capacitance of the selected ESD device should not exceed 10pF. A 0-ohm resistor can also be placed in series between the module and (U)SIM card for debugging purposes. 33pF capacitors should be connected in parallel on the USIM_DATA, USIM_CLK, and USIM_RST lines to filter out RF interference. Peripheral components of the (U)SIM card holder should be placed as close as possible to the (U)SIM card holder.

- Adding a pull-up resistor to USIM_DATA can help improve the anti-interference ability of the (U)SIM card. It is recommended to reserve a pull-up resistor near the (U)SIM card slot when the (U)SIM card traces are too long or when the interference source is close.

4.5 I2C interface

The NE26U-CN module provides a set of I2C interfaces, with a maximum speed of up to 3.4Mbps.

Table 4-7 I2C Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical Value (V)	Maximum value (V)	Note
158	I2C_SCL	OD	I2C clock signal	External 1.8 V pull-up required.				If not used, leave floating
159	I2C_SDA	OD	I2C data signal	External 1.8 V pull-up is needed.				If not used, leave floating

The I2C interface schematic diagram is as shown in the figure below, attention should be paid to level matching when designing the principle:

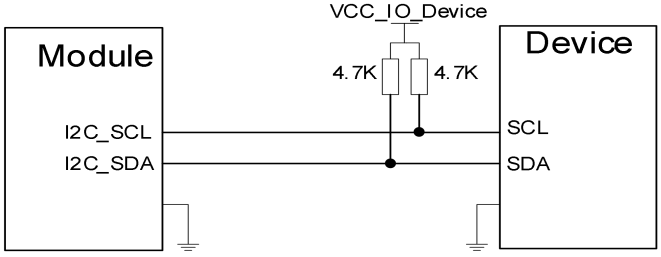


Figure 4.11 I2C Reference Design

4.6 PCM/I2S and SPI interfaces

The NE26U-CN module has 1 set of PCM interface and 1 set of I2S interface. It supports external Codec chip connection via PCM or I2S and SPI interfaces, or connects to LE9643 SLIC via PCM.

Table 4-8 PCM/I2S and SPI Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
111	PCM_DIN	DI	PCM data input	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
110	PCM_DOUT	DO	PCM data output	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
112	PCM_SYNC	DO	PCM synchronous output	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
113	PCM_CLK	DO	PCM clock output	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
18	I2S_DIN	DI	I2S data input	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
17	I2S_DOUT	DO	I2S data output	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
20	I2S_WS	DO	I2S synchronous output	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
19	I2S_CLK	DO	I2S clock output	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
170	SPI_CS	DO	SPI chip select	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
172	SPI_MISO	DI	SPI input	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
169	SPI_CLK	DO	SPI Clock	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
171	SPI_MOSI	DO	SPI output	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
200	EXT_RST	DO	External audio reset	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
199	EXT_INT	DI	External audio interruption	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
107	I2S_MCLK*	DO	I2S Master Clock Output signal	VOH	1.62	1.85	1.98	Do not open by default. Optional use
				VOL	0	-	0.18	

Note

*Indicates that the interface function is under development and not yet supported. If you need to use it, please contact our FAE for confirmation.

The external Codec device schematic is shown in the following figure, detailed design can be found in the NE26U_CN reference design:

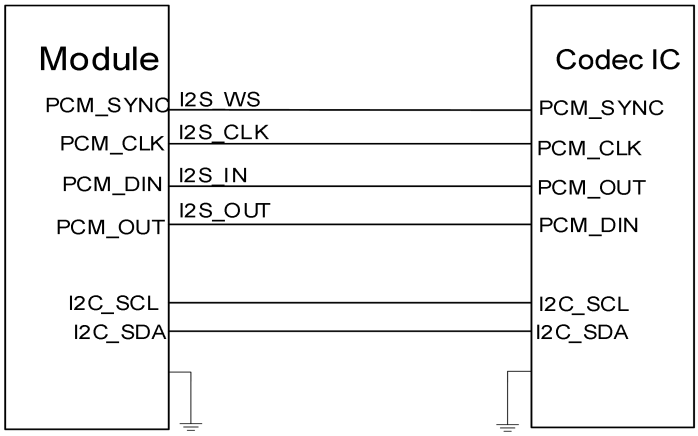


Figure 4.12 PCM/I2S External Codec Reference Design

The external SLIC device schematic diagram is shown in the figure below, detailed design can be found in the NE26U_CN reference design:

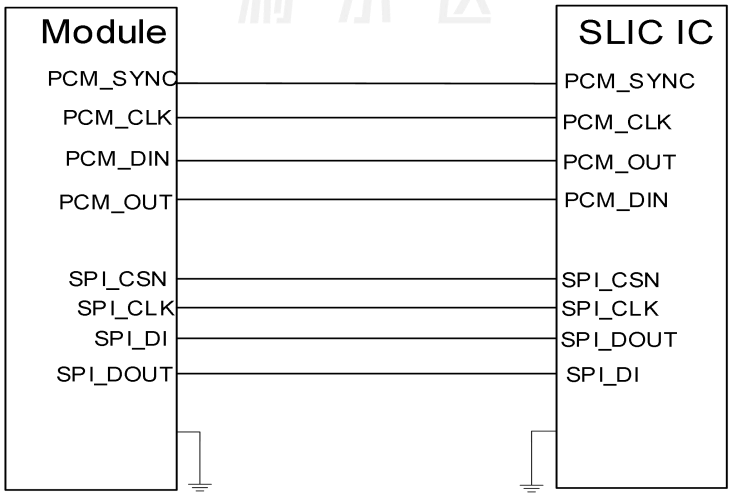


Figure 4.13 Reference Design of PCM and SPI External SLIC

Note

I2S and PCM cannot work simultaneously, the platform restriction only allows one of them to work. That means when PCM is in use, I2S cannot be used, and when I2S is in use,

PCM cannot be used.

Detailed connection of Codec or SLIC circuit can be found in the hardware reference design of NE26U-CN.

4.7 ADC interface

The NE26U-CN module provides 2 channels of analog-to-digital conversion output interfaces. To ensure the accuracy of ADC voltage detection, grounding treatment is required in the wiring. The ADC sampling accuracy is 12 bits.

Table 4-9 ADC Interface Description

Pin number	Pin Names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
12	ADC0	AI	ADC0	Voltage	0	-	VBAT	If not used, leave floating
13	ADC1	AI	ADC1	Voltage	0	-	VBAT	

Note

The ADC sampling precision is 12 bits.

The ADC input voltage must not exceed VBAT, otherwise the module will be damaged.

When VBAT voltage is off, voltage must not be applied to the ADC interface.

4.8 Status indicator interface

4.8.1 Network status indicator

The NE26U-CN module indicates the network status of the module through the NET_MODE and NET_STATUS pins, as shown in the table below.

Table 4-10 Network Status Indicator Pin Description

Pin number	Pin Name	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
203	NET_MODE	DO	Network registration indication.	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	

119	NET_STATUS	DO	Network status indicator	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	

Table 4-11 Network Status Indicator Description

Pin names	Pin working status	Network status
NET_MODE	High level	Register network status
	Low level	Other
NET_STATUS	Slow Flash (200 ms high/1800 ms low)	Check network status.
	Slow Flash (1800 ms high/200 ms low)	Standby mode
	Quick Flash (125 ms high/125 ms low)	Data transmission mode
	High level	During the call

The reference circuit is as follows:

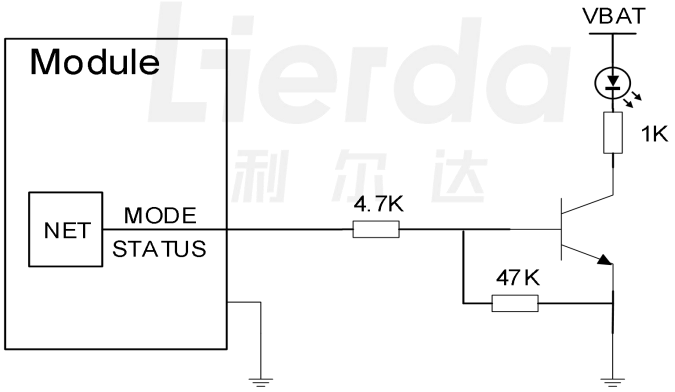


Figure 4.14 Network status indicator reference circuit

4.8.2 Module operating status indicator

The NE26U-CN module indicates the status of the module through the STATUS pin to show whether the module is in normal operation, as detailed in the table below.

Table 4-12 Running Status Indicator Pin Description

Pin number	Pin Names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
118	STAT	D	Module operating	VOH	1.62	1.85	1.98	If not used,

				VOL	0	-	0.18	

Table 4-13 Description of STATUS Work Status

Pin names	Pin working status	Network Status
STATUS	High level	The module is operating normally.
	Low level	Other

Refer to the circuit as well as the network status indicator circuit.

4.8.3 Sleep status indicator

The NE26U-CN module indicates whether the module is in sleep mode via the SLEEP_IND pin, as shown in the table below.

Table 4-14 Sleep Indicator Pin Description

Pin number	Pin names	Description	Parameters	Minimum value (V)	Maximum value (V)
156	SLEEP_IND	Module sleep status indicator	VOH	1.62	1.98
			VOL	0	0.18

Table 4-15 Description of SLEEP_IND Working States

Pin names	Pin working status	Network status
SLEEP_IND	High level	The module is in sleep mode.
	Low level	The module is in wake-up state.

Refer to the circuit as well as the network status indicator circuit.

4.8.4 MAIN_RI

MAIN_RI can have multiple indication methods as an indication signal, the default indication method is as follows:

Table 4-16 Explanation of MAIN_RI Indication Status

Pin names	Pin working status	Network status
MAIN_R	High level	Idle

Pin names	Pin working status	Network status
I	Low level	When the new URC returns, MAIN_RI will have a low level of 1S.

4.9 USB_BOOT interface

The NE26U-CN module supports the USB_BOOT function, which means that before powering on, the USB_BOOT is connected to VDD_EXT to put the module into emergency download mode. In the download mode, the module firmware can be upgraded via USB 2.0.

Table 4-17 USB_BOOT Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
168	USB_BOOT	DI	Emergency download mode	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	

The following is the reference circuit of the USB_BOOT interface:

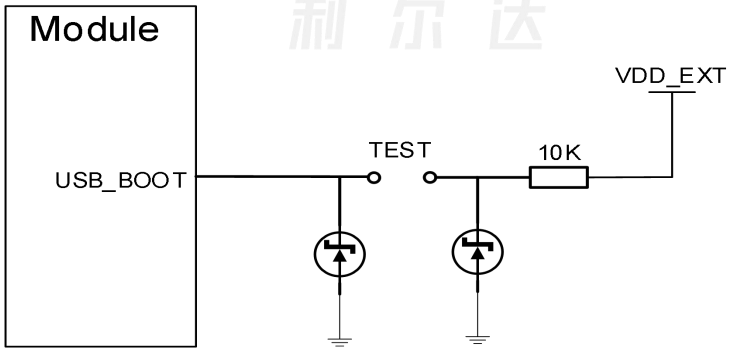


Figure 4.15 Reference Circuit for USB_BOOT Interface

4.10 WIFI control interface

The module reserves 4 WIFI control interfaces to achieve low-cost WIFI usage. 32K has output by default for direct use. 26M is closed by default, and the development of WCI coexistence serial port function is in progress. Please contact our FAE if you need to use these two functions.

Table 4-18 WIFI Control Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value	Note
1	WLAN_SLP_32K	AO	WLAN sleep clock	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
206	WLAN_EN	DO	Enable WIFI	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
207	WLAN_PWR_EN1	DO	Control WLAN FEM power supply	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
208	WLAN_PWR_EN2	DO	Control WLAN other power supply	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
48	WLAN_26M*	AO	WLAN operating clock	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
98	WCI_RX*	DI	WIFI coexist serial reception	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
99	WCI_TX*	DO	WIFI coexistence serial transmission	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
192	N79_LNA_disable*	DO	Coexistence Control	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	

Note

The interface function is under development and not yet supported. Please contact our FAE for further assistance if needed.

4.11 Antenna Tuner Control Interface*

The NE26U-CN module provides 3 GRFC RF control GPIOs and reserves 1 MIPI pin for antenna tuning switch, as defined in the table below.

Table 4-19 Antenna Tuner Control Pin Description

Pin number	Pin names	Type	Describe	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
36	GRFC1*	DO	Universal Radio Frequency Control	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
37	GRFC2*	DO	Universal Radio Frequency Control	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
38	GRFC3*	DO	Universal Radio Frequency Control	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
102	RFFE_CLK*	DO	RFFE MIPI Clock	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
103	RFFE_DATA*	DIO	RFFE MIPI Data	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
				VIH	1.26	1.85	1.98	
				VIL	0	-	0.54	

Note

*The interface function is under development and not yet supported. Please contact our FAE for further assistance if needed.

4.12 B code time synchronization interface*

The NE26U-CN module provides a B-code timing interface, which outputs the B-code signal, with pin definition and PIN36 GRFC1 multiplexing. If you need to use this function, please contact our FAE for communication.

Note

The interface function is under development and not supported at the moment. Please

contact our FAE for confirmation if needed.

4.13 LED interface

The NE26U-CN module reserves 3 LED SINK pins for driving LEDs, allowing a maximum input current of 20mA through these 3 pins.

Table 4-20 LED Interface Description

Pin number	Pin names	Category	Description	Parameters	Note
14	LED0	AI	Implement SINK current injection to light up the LED. Specific lighting states can be customized.	The maximum sink current is 20mA.	
32	LED1	AI			
33	LED2	AI			

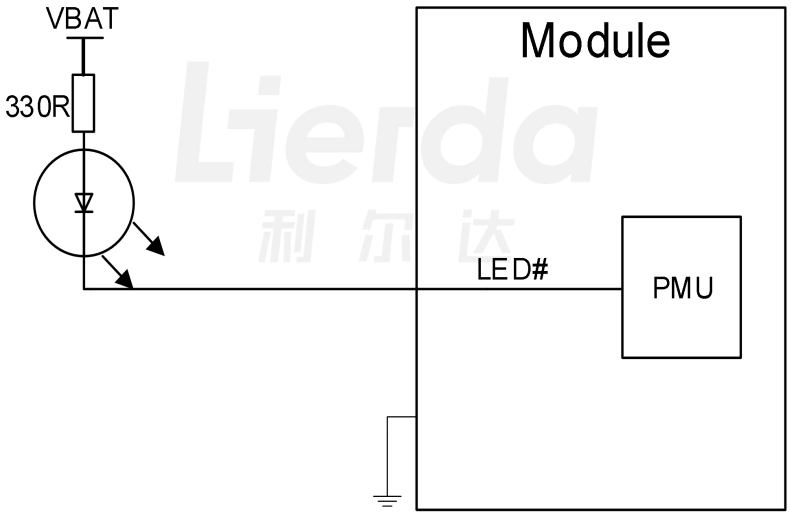


Figure 4.16 LED interface reference circuit

4.14 Charging expansion interface*

NE26U-CN module reserves 4 charging control interfaces by default, which are not used. Please consult our FAE if you need to use them.

Table 4-21 Charging Expansion Interface Description

Pin number	Pin Names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
43	BAT_DET*	AI	Battery insertion detection	VIH	1.26	1.85	1.98	If not used, leave floating
				VIL	0	-	0.54	
44	CHG_PD*	DO	External charging enable	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
45	USB_CC1*	AIO	Charging CC identification	-	0	-	VBAT	
46	USB_CC2*	AIO	Charging CC identification	-	0	-	VBAT	

Note

*Indicates that the interface function is under development and is not supported at the moment. Please contact our FAE for confirmation if needed.

4.15 GPIO interface

The NE26U-CN module reserves multiple GPIO pins for customer expansion use. The pin list is as follows, specific usage methods can be consulted with our FAE.

Table 4-22 GPIO Interface Description

Pin number	Pin name	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
204	GPIO8	DO	Universal IO control	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
117	GPIO18	DO	General IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
115	GPIO19	DO	Universal IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
179	GPIO26	DO	General IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
205	GPIO28	DO	Universal IO	VOH	1.62	1.85	1.98	

Pin number	Pin name	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
				VOL	0	-	0.18	
161	GPIO32	DO	General IO control	VOH	1.62	1.85	1.98	If not used, leave floating
				VOL	0	-	0.18	
157	GPIO33	DO	General IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
146	GPIO89	DO	Universal IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
145	GPIO90	DO	Universal IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
114	GPIO94	DO	Universal IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
202	GPIO95	DO	General IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	
104	GPIO154	DO	Universal IO control	VOH	1.62	1.85	1.98	
				VOL	0	-	0.18	

4.16 Other function interfaces

The NE26U-CN module is designed with 1 WPS function control and factory reset pin, which customers can use directly for convenient product design. It also reserves 1 set of JTAG interface for future troubleshooting.

Table 4-23 Description of Other Functional Interfaces

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Maximum value (V)
214	WPS	DI	WPS function	VIH	1.26	1.98
				VIL	0	0.54
116	Factory_RST	DI	Restore factory settings	VIH	1.26	1.98
				VIL	0	0.54
15	MTCK	DI	JTAG testing Clock input	VIH	1.26	1.98
				VIL	0	0.54
16	MTMS	DI	JTAG test module Formula Selection	VIH	1.26	1.98
				VIL	0	0.54

4.17 Antenna interface

The NE26U-CN module is designed with 4 antennas, corresponding to module pins ANT0, ANT1, ANT2, ANT3, with antenna port impedance of 50Ω.

4.17.1 Pin description

Table 4-24 Antenna Interface Pin Definitions

Pin names	Pin number	LTE WCDMA	5G NR				Frequency range
			n5/8/28	n1	n41	N77/78/79	
ANT0	54	LMHB TRX	TRX	TRX	TRX1	DRX1	703～5000
ANT1	64	—	—	DMIMO	DRX1	TRX1	2110～5000
ANT2	82	—	—	PMIMO	TRX0	DRX0	2110～5000
ANT3	90	LMHB DRX	DRX	DRX	DRX0	TRX0	703～5000

4.17.2 Antenna reference circuit

The antenna connection reference circuit for ANT0~ANT3 is shown in the following figure. The routing should be as short as possible, and at least a Π-type matching circuit should be reserved for debugging to ensure a 50Ω impedance for the routing.

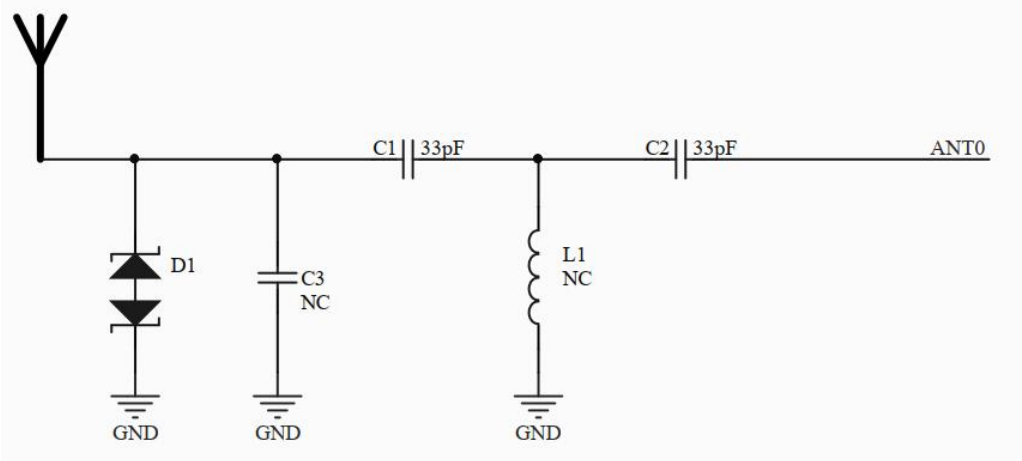


Figure 4.17 Antenna Matching Circuit

4.17.3 RF connector dimensions

The module antenna connector dimensions are as shown in the figure below:

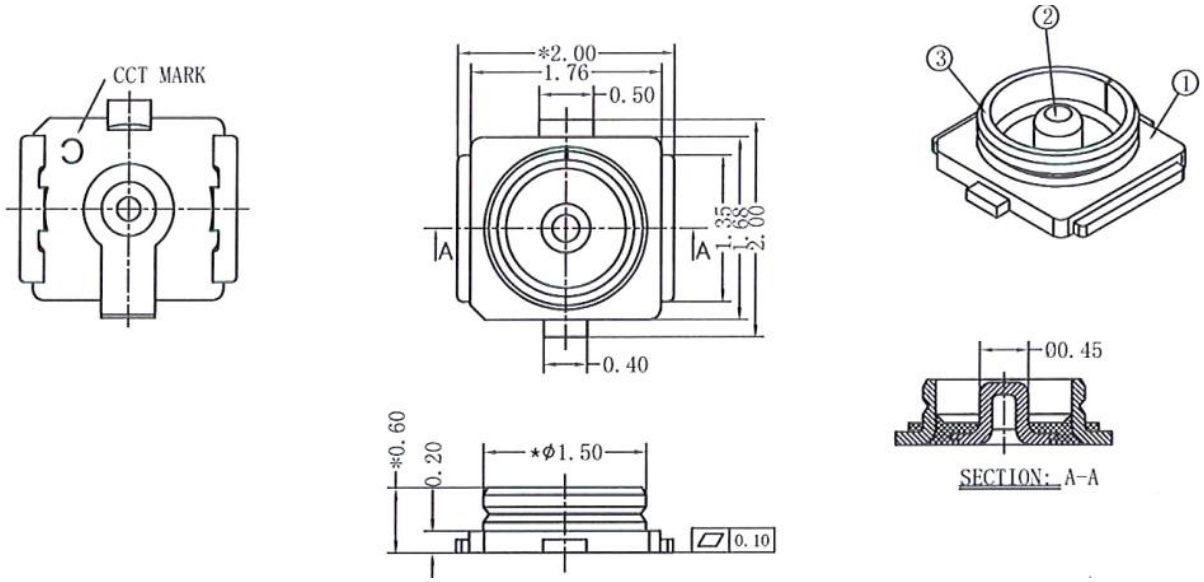


Figure 4.18 Motherboard RF connector dimension diagram (unit: mm)

Table 4-25 Main Characteristics of RF Connectors

Parameters	Standard
Nominal frequency range	DC~6GHz
Characteristic Impedance	50Ω
Temperature range	-40~90℃
Voltage Standing Wave Ratio (VSWR)	Maximum 1.3 (0~3 GHz); Maximum 1.4 (3~6 GHz)

4.17.4 RF coaxial cable requirements

Select the coaxial cable that matches the RF connector according to the following specifications.

Table 4-26 RF Coaxial Line Characteristics

Parameters	Standard
Nominal frequency range	DC~6GHz
Line Loss	0.1dBm/V@100MHz
Characteristic impedance	50Ω
Temperature range	-40~85℃

Voltage Standing Wave Ratio (VSWR)	Maximum 1.5 (3-6 GHz)

The figure shows the post-assembly states of 0.81 fourth-generation end cap and 1.13 fourth-generation end cap.

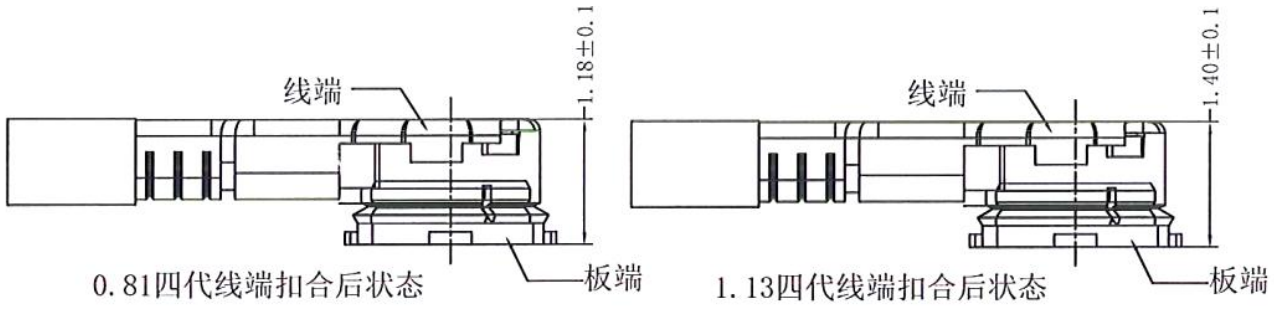


Figure 4.19 Status after the cable connector is fastened.

4.17.5 Antenna selection requirements

The passive parameters selection of the antenna are as follows.

Table 4-27 Antenna Selection Parameters

Parameters	Standardized
Characteristic impedance	50Ω
Standing wave ratio	≤ 2
Efficiency	> 30%
Insertion	Low frequency: <1dB, mid frequency: <1.5dB, high frequency:

Passive parameters are for reference only, actual selection should be based on OTA data.

5 Radio Frequency Characteristics

This chapter mainly introduces the RF characteristics of the module:

- Conduction reception sensitivity
- Transmitting power

5.1 Conduction test data

5.1.1 Test environment

Test equipment: CMW500, MT8000A

Power: 66319D

5.1.2 Conductive reception sensitivity

The reception sensitivity index is an important parameter for measuring the performance of the NE26U-CN module, and the test results are shown in the table below.

Table 5-1 Description of Reception Sensitivity

Frequency band	Test value (unit: dBm)			3GPP(SIMO)
	Main set	Episode	SIMO[1]	
WCDMA Band 1	-109	-109.5	-112	-106.7
WCDMA Band 5	-108	-110	-111.5	-104.7
WCDMA Band 8	-109.5	-110	-112.8	-103.8
LTE Band 1(10 MHz)	-98.6	-98.2	-100.8	-96.3
LTE Band 3(10 MHz)	-97.5	-97	-100	-93.3
LTE Band 5(10 MHz)	-97	-98.8	-101	-94.3
LTE Band 8(10 MHz)	-98.5	-98.8	-101.5	-93.3
LTE Band 34(10 MHz)	-96.5	-97	-99.5	-96.3
LTE Band 38(10 MHz)	-98.2	-98.3	-101.2	-96.3

[1] 对于 SIMO 灵敏度测试值，WCDMA、LTE、NR n5/n8/n28 是在 2RX 天线下测量得到，NR n1/n41/n77/n78/n79 是在 4RX 天线下测量得到。

Frequency band	Test value (unit: dBm)			3GPP(SIMO)
	Main set	Episode	SIMO[1]	
LTE Band 39(10 MHz)	-97.5	-97	-100.2	-96.3
LTE Band 40(10 MHz)	-98	-97	-100.5	-96.3
LTE Band 41(10 MHz)	-96.5	-98	-99.5	-94.3
NR n1(10 MHz)	/	/	-105	-99.5
NR n5(10 MHz)	/	/	-99	-94.8
NR n8(10 MHz)	/	/	-100.5	-93.8
NR n28(10 MHz)	/	/	-101	-95.5
NR n41(100 MHz)	/	/	-92	-87.2
NR n77(100 MHz)	/	/	-93.5	-87.7
NR n78(100 MHz)	/	/	-93.6	-88.2
NR n79(100 MHz)	/	/	-94	-88.3

5.1.3 Transmitting power

The transmission power is an important indicator for measuring the performance of the NE26U-CN module, and the test results are shown in the table below.

Table 5-2 Power Transmission Description

Frequency band	Maximum value of transmission power	Minimum value of transmission power
WCDMA B1/B5/B8	24dBm +1.7/-3.7dB	< -49dBm
LTE	23dBm ±2.7dB	< -39dBm
NR n1/n5/n8/n41	23dBm ±2.7dB(Class 3)	< -40dBm
NR n28	23dBm +2.7/-3.2dB(Class 3)	< -40dBm
NR n77/n78/n79	23dBm +2.7/-3.7dB(Class3)	< -40dBm
NR n41/n77/n78/n79	26dBm +2.7/-3.7dB(Class2)	< -40dBm

6 Electrical performance and reliability

This chapter mainly introduces the electrical characteristics and reliability characteristics of the NE26U-CN module interface.

6.1 Work and storage environment

The operating and storage temperature ranges of the NE26U-CN module are shown in the table below.

Table 6-1 Working and Storage Temperatures

Parameters	Minimum value (° C)	Maximum value (° C)
Normal operating temperature	-30	+75
Expand operating temperature.	-40	+85
Storage temperature	-40	+90

6.2 Rated power value

The input voltage requirements for the NE26U-CN module are as shown in the table below.

Table 6-2 Operating Voltage

Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Ripple (V)
VBAT_BB	3.3	3.8	4.3	≤0.1
VBAT_RF	3.3	3.8	4.3	≤0.1

6.3 Absolute maximum rating

Table 6-3 Absolute Maximum Ratings

Parameters	Minimum value (V)	Maximum value (V)
VBAT	-0.3	6
Digital interface voltage	-0.3	2.1

6.4 Power consumption characteristics

Table 6-4 Power Consumption of the Module

Module status	Condition	Average Typ.Current(mA)@ 3.8V
Shutdown mode	Module power OFF	0.059
Sleep mode	Idle(AT+cfun=0)	3.15
Maximum transmission power of WCDMA	WCDMA B1 HSDPA CH9750 @ 23.05 dBm	631
	WCDMA B5 HSDPA CH4182 @ 23.83dBm	537
	WCDMA B8 HSDPA CH2788 @ 23.61 dBm	580
Maximum transmission power of LTE	LTE-FDD B1 CH18300@22.32dBm	608
	LTE-FDD B3 CH19575@22.63dBm	518
	LTE-FDD B5 CH20525@23.61dBm	592
	LTE-FDD B8 CH21625@23.37dBm	549
	LTE-TDD B34 CH36275@21.78dBm	244
	LTE-TDD B38 CH38000@22.39dBm	375
	LTE-TDD B39 CH38450@22.1dBm	257
	LTE-TDD B40 CH39150@21.84dBm	308
	LTE-TDD B41 CH40620@22.08dBm	369
Maximum transmission power of 5G NR	5G NR-FDD n1 CH423000@22.51dBm	1024
	5G NR-FDD n1 CH428000@22.12dBm	993
	5G NR-FDD n1 CH429000@22.41dBm	1004
	5G NR-FDD n5 CH175800@21.57dBm	797
	5G NR-FDD n5 CH176300@21.5dBm	806
	5G NR-FDD n5 CH176800@21.94dBm	804
	5G NR-FDD n8 CH187000@22.17dBm	817
	5G NR-FDD n8 CH188500@21.42dBm	841
	5G NR-FDD n8 CH190000@21.39dBm	833
	5G NR-FDD n28 CH154600@21.39dBm	833
	5G NR-FDD n28 CH156100@21.77dBm	815
	5G NR-FDD n28 CH158600@21.68dBm	785
	5G NR-TDD n41 CH509202@26.33dBm	610
	5G NR-TDD n41 CH518600@26.29dBm	619
	5G NR-TDD n41 CH527997@26.45dBm	603
	5G NR-TDD n77 CH623334@26.18dBm	637
	5G NR-TDD n77 CH650000@26.42dBm	661
	5G NR-TDD n77 CH676666@25.96dBm	665

Module status	Condition	Average Typ.Current(mA)@ 3.8V
	5G NR-TDD n78 CH623334@25.67dBm	635
	5G NR-TDD n78 CH636667@25.69dBm	644
	5G NR-TDD n78 CH649999@25.91dBm	655
	5G NR-TDD n79 CH696668@26.35dBm	613
	5G NR-TDD n79 CH713334@25.75dBm	618
	5G NR-TDD n79 CH729999@26.14dBm	635

6.5 ESD protection

6.5.1 ESD design recommendations

The overall ESD performance is mainly determined by: structural shielding, PCB layout protection, and device protection performance. Here are some considerations for device selection:

- Reverse leakage current IR: Excessive reverse current not only increases system power consumption but may also affect signal functionality, especially more pronounced in high-speed, low-drive capability signals.
- Reverse working voltage VRWM: This voltage should be higher than the normal operating voltage at the protected network terminal;
- IPP, Clamping Voltage, and Peak Pulse Power: These three parameters follow the relationship P=UI, the lower the clamping voltage, the safer the back-end device; ESD is easily weakened by factors such as structure, PCB capacitance, etc., so the discharged static electricity will not be fully applied to the network to be protected, making it difficult to estimate these parameters;
- Interlayer capacitance CJ: Interlayer capacitance that is too large will affect the integrity of high-speed signals;

We suggest:

(1) High-speed signal interface: CJ<1pF for USB2.0 interface, CJ<0.5pF for USB3.0 interface.

(2) Low-speed signal interface: (U)SIM interface CJ<10pF, UART interface, PCM

interface CJ<20pF, TVS diode or varistor can be used for ESD protection.

- Antenna Interface: If TVS devices are used in the antenna interface, the RSE (Radiated Spurious Emissions) may exceed the values defined by EN301489. Therefore, it is not recommended to use TVS at the antenna port. It is suggested to connect an inductor of 47nH~82nH for ESD protection.

6.5.2 ESD environmental control recommendations

(1) The processing equipment, testing instruments, tools, and equipment of electrostatic sensitive components shall all be reliably grounded;

(2) Parts that come into contact with static-sensitive components on equipment, instruments, tools, and fixtures, as well as moving parts near static-sensitive components, are made of anti-static materials and are well grounded. Non-antistatic material parts are treated with antistatic measures.

(3) In the process of handling electrostatic sensitive devices such as ICs, single board, modules, etc., employees all correctly wear static wrist straps or static gloves;

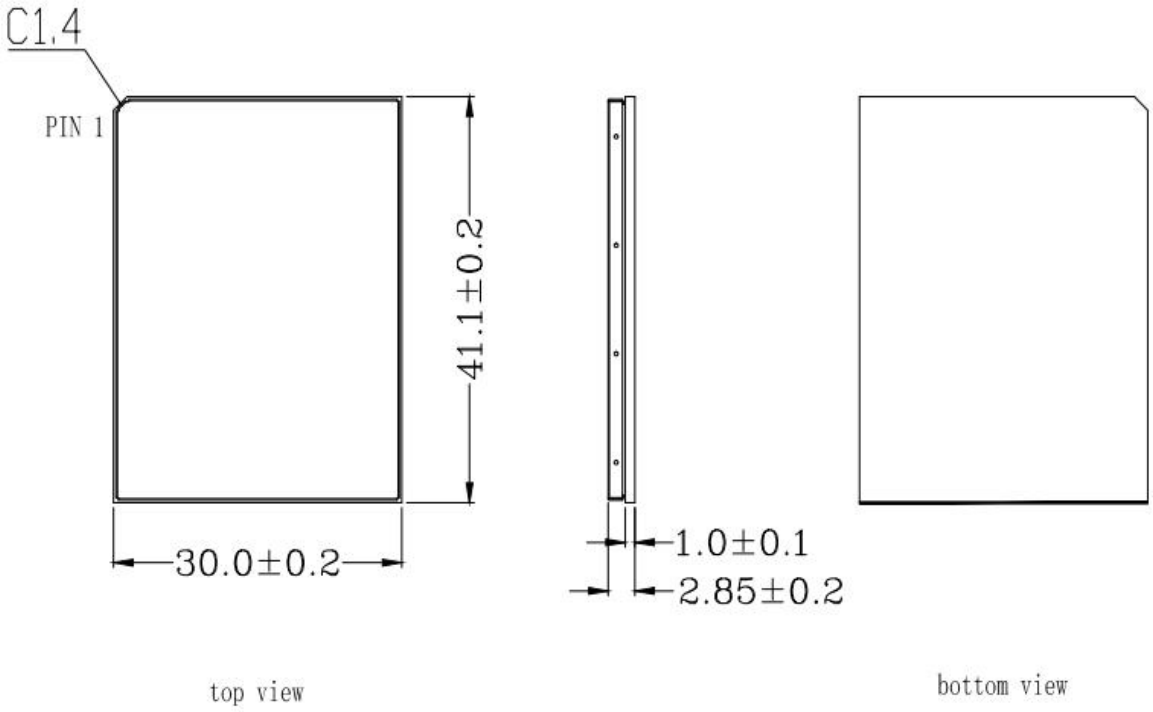
(4) Are there obvious anti-static markings and anti-static measures in the process of transporting and storing electrostatic sensitive devices?

Table 6-5 ESD performance parameters (Temperature: 25°C, Humidity: 40%)

Pin name	Discharge phenomenon	Air discharge
VBAT,GND	+/-5kV	+/-10kV
Antenna interface	+/-4kV	+/-8kV
Others	+/-0.5kV	+/-2kV

7 Structure Specifications

7.1 Mechanical dimensions



UNIT:mm

Figure 7.1 Module Mechanical Dimension Diagram

7.2 Recommend encapsulation

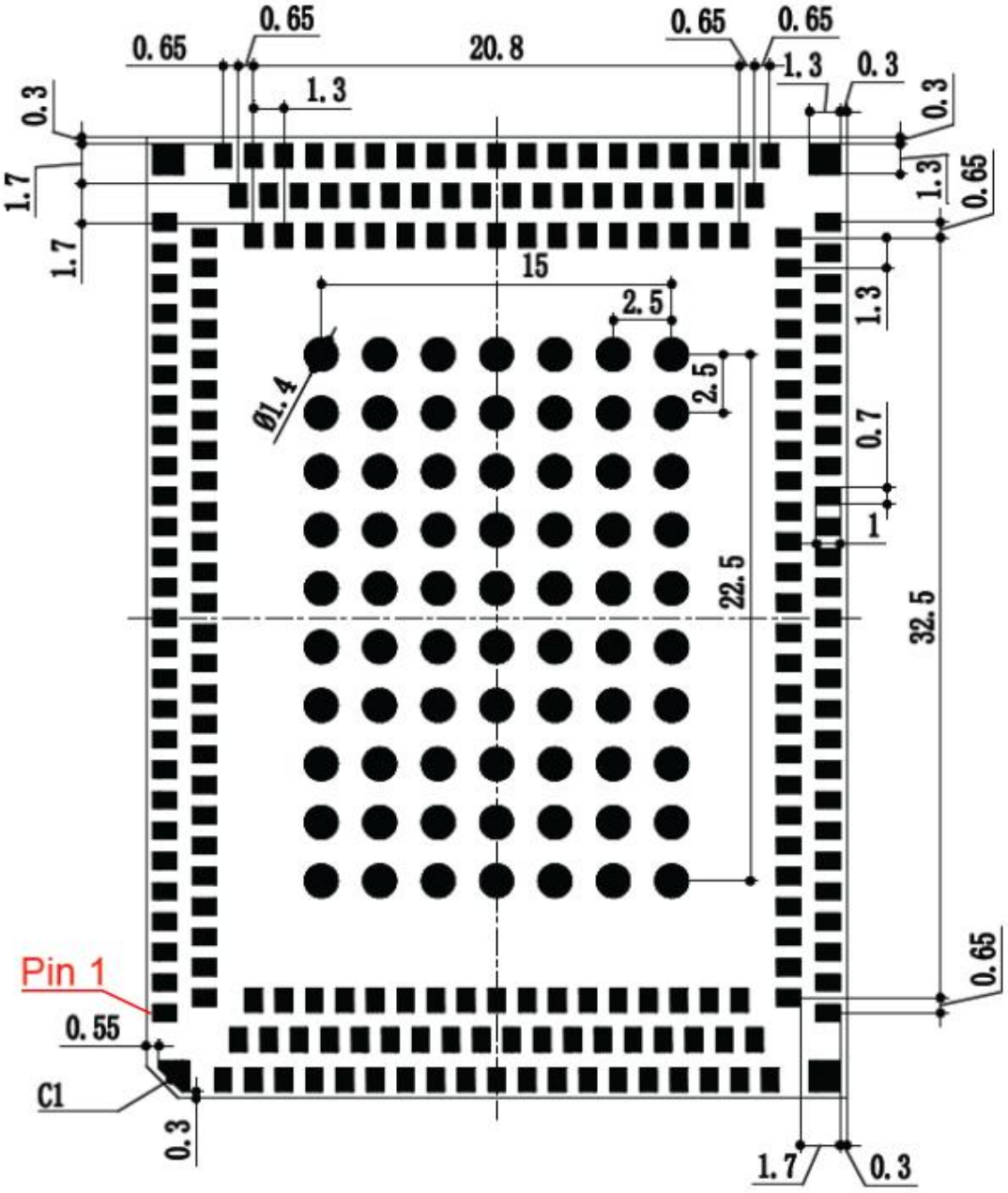


Figure 7.2 Module Recommended Package (Bottom View)

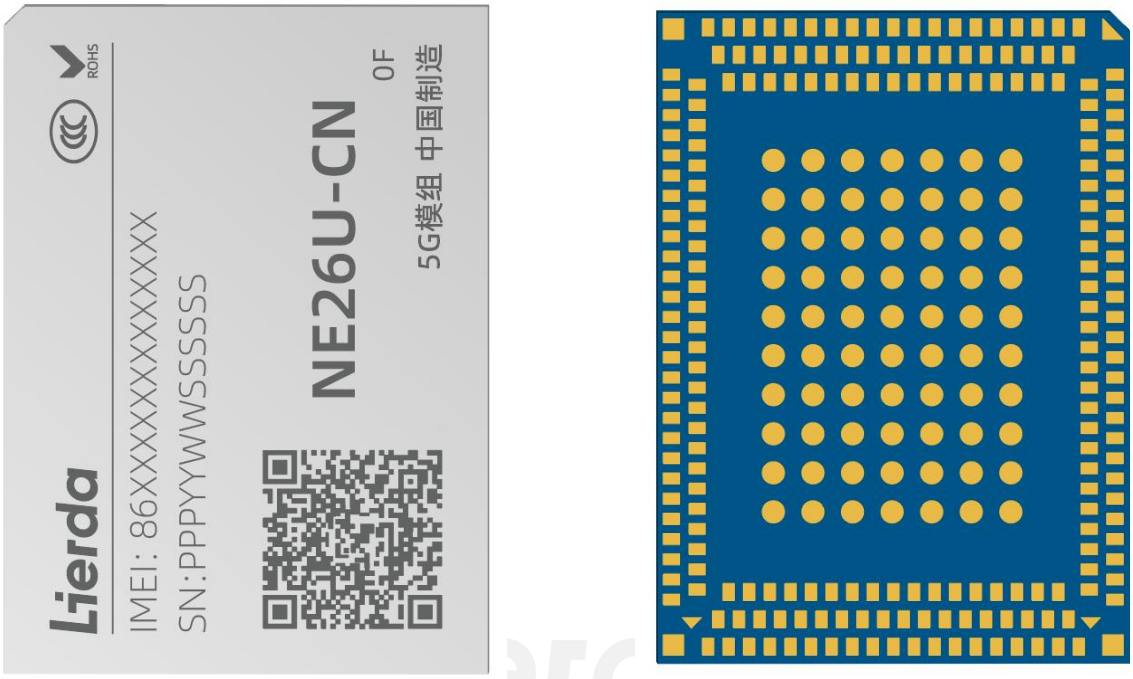
Note

To ensure the welding quality of the components and facilitate future maintenance operations, the distance between the modules on the customer's motherboard and other components should be at least 3 mm.

To ensure the reliability of pasting and welding, it is recommended that the mainboard

thickness be maintained at least 1.2 mm.

7.3 Module effect diagram



Top View Bottom View

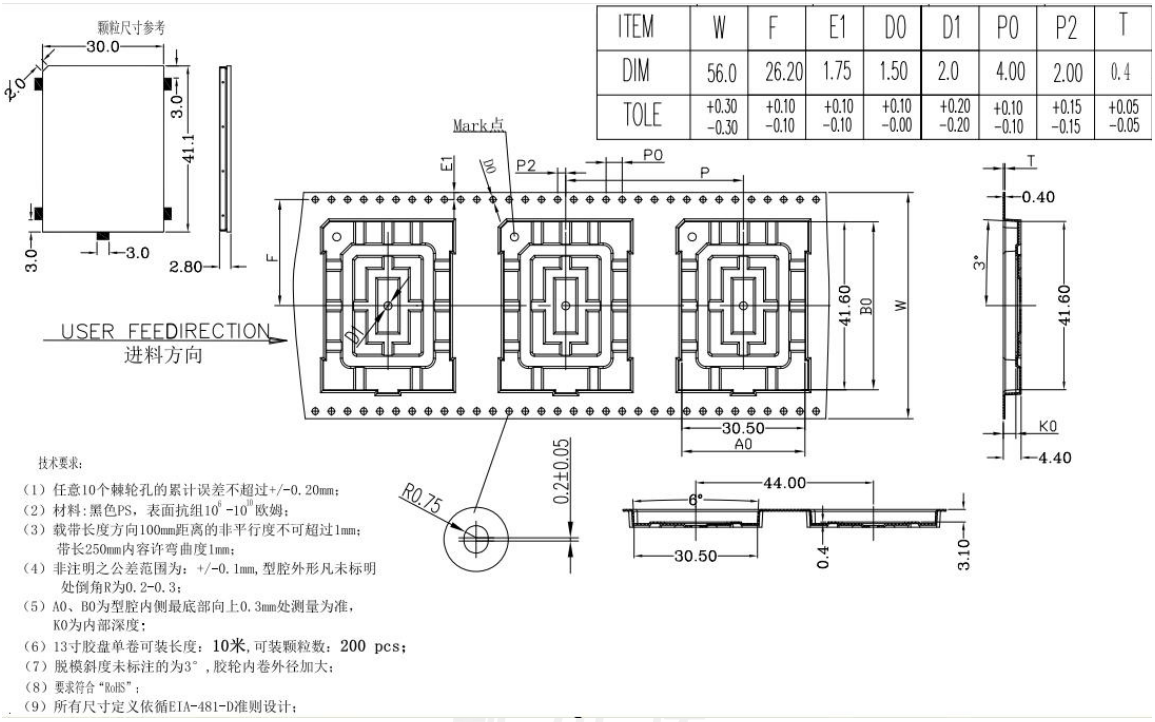
Figure 7.3 Module Top/Bottom View

The above is the design rendering of the module, please refer to the actual module for accuracy, especially the label content is for reference only.

8 Packaging information

8.1 Carrying adhesive wheel dimensions

The dimensions of the carrier are as follows:



ITEM	W	F	E1	D0	D1	P0	P2	T
DIM	56.0	26.20	1.75	1.50	2.0	4.00	2.00	0.4
TOLE	+0.30 −0.30	+0.10 −0.10	+0.10 −0.10	+0.10 −0.00	+0.20 −0.20	+0.10 −0.10	+0.15 −0.15	+0.05 −0.05

Figure 8.1 Dimensional Drawing of the Conveyor Belt (unit:mm)

The rubber wheel dimensions are as follows:

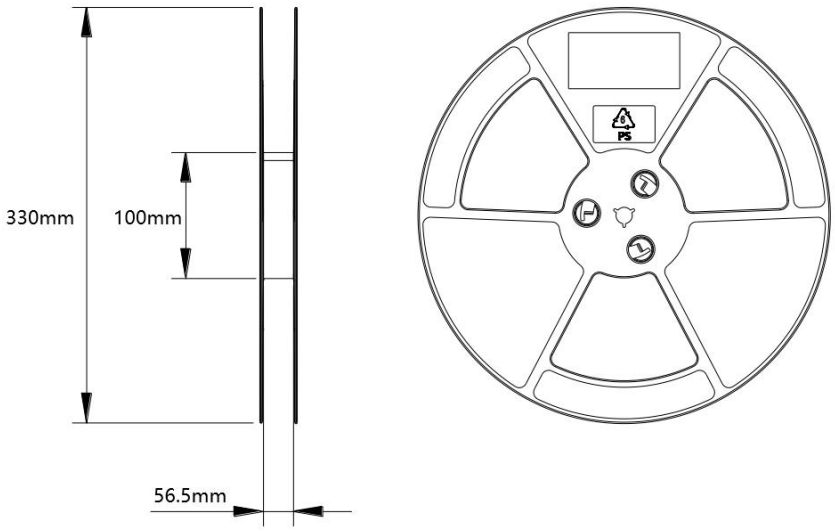
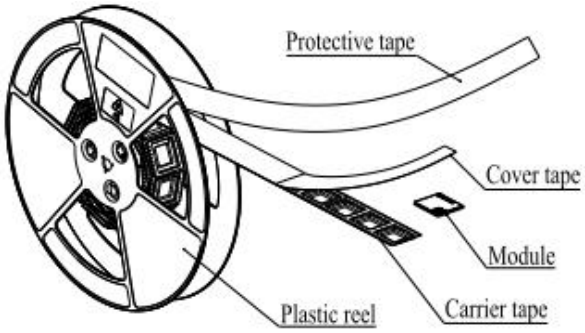


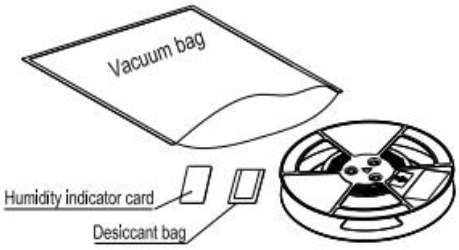
Figure 8.2 Tire Dimensional Drawing (unit:mm)

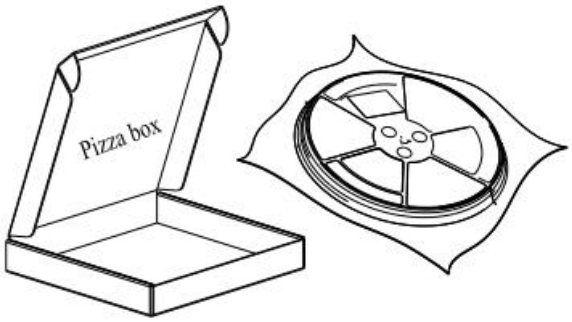
8.2 Packaging process



将模块放入载带中，使用上带热封；再将热封后的载带缠绕到胶盘中，用保护带缠绕防护。1个胶盘可装载 200 片模块。

将包装完成的胶盘、湿敏卡和干燥剂放入真空袋中，抽真空。





将抽真空后的胶盘放入披萨盒内。

将 5 个披萨盒放入 1 个卡通箱内，封箱。1 个卡通箱可包装1000片模块。

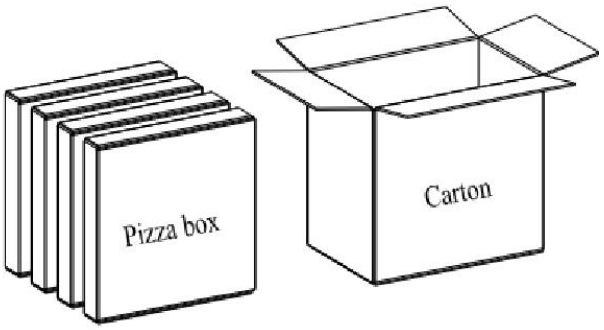


Figure 8.3 Packaging Process

9 Related documents and terminology abbreviations

Table 9-1 Related Documents

Serial number	Document name	Comments
[1]	NE26U-CN AT Command Manual V1.0	AT command set

Table 9-2 Term Abbreviations

Abbreviation	Full English name	Full name in Chinese
bps	bits per second	Per second
CPE	Customer-Premise Equipment	User's stationed equipment
FOTA	Firmware Over-The-Air	Firmware over-the-air differential upgrade
ESD	Electrostatic Discharge	Electrostatic discharge
FDD	Frequency Division Duplexing	Frequency Division Multiplexing
HSPA	High Speed Packet Access	High-speed data packet access
HSUPA	High Speed Uplink Packet Access	High-speed uplink data packet access
kbps	Kilo Bits Per Second	Thousand bits per second
LED	Light Emitting Diode	Light Emitting Diode
LTE	Long Term Evolution	Long-term evolution
Mbps	Mega Bits Per Second	Megabits per second
MIMO	Multiple-Input Multiple-Output	Multiple inputs, multiple outputs
NR	New Radio	New Air Interface
PCIe	Peripheral Component Interconnect Express	Peripheral component interconnect standard
PCM	Pulse Code Modulation	Pulse Code Modulation
PPP	Point-to-Point Protocol	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation	Orthogonal Amplitude Modulation

Abbreviation	Full English name	Full name in Chinese
QPSK	Quadrature Phase Shift Keying	Orthogonal Phase Shift Keying
RC	Root Complex	Root complex
RF	Radio Frequency	Radio Frequency
RFFE	RF Front-End	RF front end
Rx	Receive	Receive
SCS	Subcarrier Spacing	Carrier Spacing
SIMO	Single Input Multiple Output	Single Input Multiple Output
SMS	Short Message Service	Short Message Service
Tx	Transmit	Send
UART	Universal Asynchronous Receiver & Transmitter	General asynchronous transceiver
USB	Universal Serial Bus	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module	(Global) User Identification Module
VIH	Input High Voltage Level	Enter high voltage level
VIL	Input Low Voltage Level	Enter low voltage level.
VOH	Output High Voltage Level	Output high voltage level
VOL	Output Low Voltage Level	Output low voltage level
WCDMA	Wideband Code Division Multiple Access	Broadband code division multiple access.