Lierda NR90-HCN M.2 module

Hardware Design Manual

Version: Rev1.6

Date: 25/04/25

Status: Released

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Revision History of the Document

Document Version	Change date	Reviser	Reviewer	Change content
Rev1.0	23-10-16	WPL	YY，XL	Initial Version
Rev1.1	24-1-18	WPL	YY，XL	1、Update power consumption data 2、Update the transmission power and reception sensitivity data. 3、Update tray dimensions.
Rev1.2	24-05-15	WPL	YY，XL	1、Update the I2C_SCL pin number and description in Table 4-6 and Figure 4-9 of Chapter 4.5 to be consistent with the pin description table. 2、Update pin name and pin description to match in Chapter 4.6, pin 24.
Rev1.3	24-08-20	WPL	YY，XL	1、Key Features Table: Add LTE 1.8G private network frequency band to the working frequency band. 2、Update the receiving sensitivity data of the MIMO in the NR frequency band.
Rev1.4	25-01-02	WPL	YY，XL	1. Delete the information about PC2 related to N41/N77/N78. 2. Add tolerance information to the dimension drawing.
Rev1.5	25-01-04	WPL	YY，XL	1. Update the renderings.
Rev1.6	25-04-25	WPL	YY，XL	Standardization optimization of documents

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Safety first when driving! Do not use hand-held mobile devices while driving unless they have hands-free functionality. Please pull over before making a call!

Please turn off your mobile devices before boarding. The wireless function of mobile devices is prohibited from being turned on in the airplane to prevent interference with the aircraft communication system. Ignoring this prompt may jeopardize flight safety or even violate the law.

When in a hospital or healthcare facility, pay attention to any restrictions on the use of mobile terminal devices. RF interference can cause medical equipment to malfunction, so it may be necessary to turn off mobile terminal devices.

Mobile terminal devices do not guarantee effective connection in all circumstances, such as when there is no phone credit or the SIM card is invalid. In case of emergency situations with the above conditions, please remember to use emergency calls, and ensure that your device is powered on and in an area with sufficient signal strength.

Your mobile terminal device will receive and transmit radio frequency signals when it is powered on, which may cause radio frequency interference when near a TV, radio, computer, or other electronic devices.

Please keep mobile terminal devices away from flammable gases. When you are near gas stations, oil depots, chemical plants, or explosive operation sites, please turn off your mobile terminal devices. Operating electronic devices in any location with potential explosion hazards poses a safety risk.

Module selection for application

Serial number	Module model	Feature symbol	Support frequency band	Dimensions (mm)	Module introduction
1	NR90-HCN M.2		WCDMA/LTE/NR	30 x 52 x 3.3	5G Redcap module

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1 Introduction

This document defines the hardware application specification of the Lierda Group's NR90-HCN M.2 5G Redcap module, describing its hardware interface, electrical characteristics, application methods, and mechanical specifications.

This document can help users quickly understand the hardware interface specifications, electrical, mechanical characteristics, and other related information of the module. Combined with other relevant documents, users can quickly grasp the application methods of the module.

2 Product Overview

Lierda NR90-HCN M.2 5G Redcap module is based on 3GPP Release 17 technology, supporting 5G standalone networking (SA) mode, compatible with 4G network standards, meeting the frequency band requirements of the four major domestic operators, covering some overseas regional frequency bands, and supporting 1.8GHz industrial private networks.

NR90-HCN M.2 module uses M.2 Key B interface, with dimensions of 30*52*3.3mm, easy to install.

The NR90-HCN M.2 module can be compatible with various types of operating systems (Android, Linux, Windows, etc.), support multiple drivers and network protocols, and can provide voice functions to meet different application scenarios.

Lierda NR90-HCN M.2 module is designed for high-reliability, low-latency, large connectivity, and high-capacity application scenarios for 5G RedCap modules. With a smaller size, lower power consumption, and fewer antennas, the NR90-HCN M.2 module will better support the rapid commercialization of RedCap technology.

2.1 Frequency bands and functions

The frequency bands supported by the NR90-HCN M.2 module are as shown in the table below:

Table 2-1 Description of frequency bands supported by NR90-HCN M.2 module

Frequency band	Launch	Receive
WCDMA Band 1	1920MHz-1980MHz	2110MHz-2170MHz
WCDMA Band 5	824MHz-849MHz	869MHz-894MHz
WCDMA Band 8	880MHz-915MHz	925MHz-960MHz
FDD LTE Band 1	1920MHz-1980MHz	2110MHz-2170MHz
FDD LTE Band 3	1710MHz-1785MHz	1805MHz-1880MHz
FDD LTE Band 5	824MHz-849MHz	869MHz-894MHz
FDD LTE Band 8	880MHz-915MHz	925MHz-960MHz
TDD LTE Band 34	2010MHz-2025MHz	2010MHz-2025MHz
TDD LTE Band 38	2570MHz-2620MHz	2570MHz-2620MHz
TDD LTE Band 39	1880MHz-1920MHz	1880MHz-1920MHz
TDD LTE Band 40	2300MHz-2400MHz	2300MHz-2400MHz
TDD LTE Band 41	2496MHz-2690MHz	2496MHz-2690MHz
NR n1	1920MHz-1980MHz	2110MHz-2170MHz
NR n3*	1710MHz-1785MHz	1805MHz-1880MHz
NR n5*	824MHz-849MHz	869MHz-894MHz
NR n8	880MHz-915MHz	925MHz-960MHz
NR n28	703MHz-748MHz	758MHz-803MHz
NR n41	2496MHz-2690MHz	2496MHz-2690MHz
NR n78	3300MHz-3800MHz	3300MHz-3800MHz
NR n79	4400MHz-5000MHz	4400MHz-5000MHz

NR90-HCN M.2 module can be applied in the following terminal scenarios:

- Intelligent Industry
- Energy and power
- Video surveillance

- Mobile broadband
- Connected Vehicles
- Smart wearables

2.2 Key Features

The table shows the main features of the NR90-HCN M.2 module.

Table 2-1 Main Features of the NR90-HCN M.2 Module

Type	Describe
Encapsulation	M.2 Key B
Physical properties	Dimensions: 30 x 52 x 3.3mm Weight: about 9.6g
Working frequency band	5G SA: n1/n3*/n5*/n8/n28/n41 (all bands)/n78/n79 LTE FDD：B1/B3/B5/B8 LTE TDD: B34/B38/B39/B40/B41 (full band) LTE 1.8G private network: B59/B62 WCDMA：B1/B5/B8
Transmission rate (theoretical value)	SA DL：220Mbps；UL：110Mbps LTE DL：192Mbps；UL：98Mbps WCDMA DL：384kbps；UL：384kbps
Power level	WCDMA：Class 3 LTE：Class 3 LTE B41：Class 2 5G NR n1/n3*/n5*/n8/n28/n41：Class 3 5G NR n78/n79：Class 3 5G NR n41/n78/n79 HPUE
WCDMA features	Support 3GPP FDD R6 version protocol Maximum transmission rate (theoretical value): WCDMA: 384kbps (downlink speed) / up to 384kbps (uplink speed)
LTE features	Support 3GPP R13 protocol version Support LTE FDD/TDD. Support CAT4 Support 1.4/3/5/10/15/20 MHz RF bandwidth. Support uplink QPSK, 16QAM, 64QAM, 256QAM modulation schemes. Support QPSK, 16QAM, 64QAM, 256QAM modulation schemes. Support downlink 2×2 MIMO.

Type	Describe
	Maximum transmission rate (theoretical value): LTE: 192Mbps (downlink speed) / 98 Mbps (uplink speed)
5G NR features	Support 3GPP R17 protocol version Support uplink 256QAM modulation and downlink 256QAM modulation. Lierda n1/n3*/n5*/n8/n28/n41/n78/n79 support downlink 2×2 MIMO Support 15kHz and 30kHz for SCS. Support SA working mode Support Option 3x, 3a, 3 and Option 2 Maximum transmission rate (theoretical value, related to network configuration and heat dissipation environment): SA: 220Mbps (downlink speed) / 110Mbps (uplink speed)
Operating voltage range	DC 3.3V ~ 4.4V (typical value 3.8V)
Application temperature range	Operating temperature: -30 ~ +75°C Operating Temperature: -40 ~ +85°C Storage temperature: -40 ~ +90°C
AT command	Refer to the detailed design document of AT command NR90-HCN.
USB interface	USB2.0 (High Speed) interface, with a maximum speed of 480Mbps.
UART interface	2-line UART
(U)SIM interface	2 standard SIM interfaces (Class B and Class C) Support dual SIM dual standby.
PCM	Support voice
I2C interface	Support standard mode and quick mode.
PCIe interface	Compliant with PCIe 1.1 specification, transfer rate can reach 2.5Gbps.
Time service interface	IRIG_B*1；1PPS*1
Control Interface	POWER_ON_OFF# W_DISABLE# WOWWAN# WAKE_IN RESET#
Antenna interface	ANT*2
Network Protocol	PPP/RNDIS/ECM

Type	Describe
	TCP/IP MQTT
Drive	Linux Windows XP/7/8/10 Andriod
AT	Support AT commands compliant with 3GPP standards.
FOTA	Support
OneNET	Support
Certification	CCC/SRRC/NAL/CE/Operator Certification* (Telecom/Unicom/Mobile)

Note

Under development, N3/N5 indicates N3/N5 certification in progress.

2.3 Function Block Diagram

The diagram illustrates the main functions of the NR90-HCN M.2 module: power management, baseband section, memory, RF functional blocks, peripheral interfaces.

Figure 2.1 NR90-HCN M.2 Module Hardware Block Diagram

2.4 Pinout diagram

The following is the pin assignment diagram for the NR90-HCN M.2 interface.

No.	Pin Name	Pin Name	No.
74	VBAT	CONFIG_2	75
72	VBAT	GND	73
70	VBAT	GND	71
68	I2C_SDA	CONFIG_1	69
66	USIM0_DETECT	RESET#	67
64	UART_TXD	VDD_EXT	65
62	UART_RXD	PPS_OUT	63
60	I2C_SCL	NC	61
58	ANT_CTRL0	NC	59
56	ANT_CTRL1	GND	57
54	PEWAKE	REFCLKP	55
52	CLKREQ#	REFCLKN	53
50	PERST#	GND	51
48	USIM1_PWR	PERp0	49
46	USIM1_RST	PERn0	47
44	USIM1_CLK	GND	45
42	USIM1_DATA	PETp0	43
40	USIM1_DET	PETn0	41
38	WAKE_IN	GND	39
36	USIM0_PWR	NC	37
34	USIM0_DATA	NC	35
32	USIM0_CLK	GND	33
30	USIM0_RESET	NC	31
28	PCM_SYNC	NC	29
26	IRIG_B	GND	27
24	PCM_OUT	RESERVED	25
22	PCM_IN	WOWWAN#	23
20	PCM_CLK	CONFIG_0	21
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
10	LED1#	GND	11
8	W_DISABLE#	USB_DM	9
6	POWER_ON_OFF#	USB_DP	7
4	VBAT	GND	5
2	VBAT	GND	3
		CONFIG_3	1

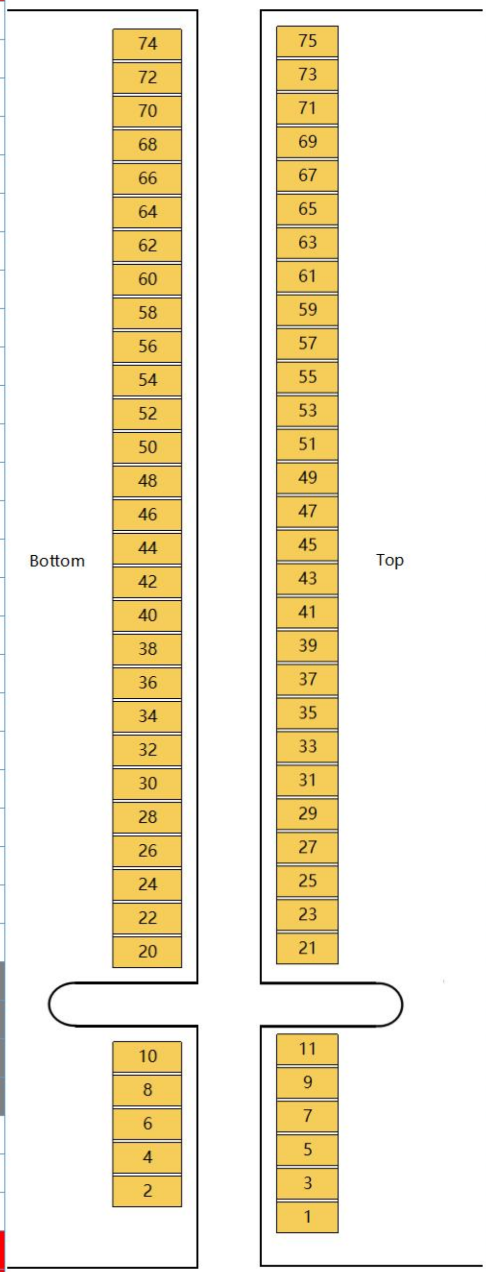


Figure 2.2 Module Pinout Diagram

2.5 Pin Description Table

Table 2-2 I/O Type Definitions

Type	Description

PI	Power input signal
PO	Power output signal
DI	Digital input signal
DO	Digital Output Signal
AI	Simulated input signal
AO	Simulate output signal
DIO	Digital bidirectional input/output signal
OD	The leakage pole opens the way
VIL	Low-level input voltage
VIH	High-level input voltage
VOL	Low-level output voltage
VOH	High-level output voltage

Table 2-3 Pin Definitions

Pin number	Pin names	Type	Description	Note
1	CONFIG_3	DO	The voltage value is determined by the host end and is used for M.2 port type	If not used, leave floating
2	VBAT	PI	Module main power supply	3.3-4.4V, typical: 3.8V
3	GND	G	GND	
4	VBAT	PI	Module main power supply	3.3-4.4V, typical: 3.8V
5	GND	G	GND	
6	POWER_	DI	Power On/Off Control	High level power on.
7	USB_DP	AIO	USB2.0 differential data (+)	
8	W_DISAB	DI	Flight mode control	If not used, leave
9	USB_DM	AIO	USB2.0 differential data (-)	
10	LED1#	OD	Module status indicator light	Maximum sink
11	GND	G	GND	
12～19	Groove	Groove		
20	PCM_CLK	DIO	PCM clock	If not used, leave
21	CONFIG_0	DO	The voltage value is determined by the host end for M.2 port type identification.	If not used, leave floating
22	PCM_IN	DI	PCM data input	If not used, leave

Pin number	Pin names	Type	Description	Note
23	WOWWA	DO	Wake up the host	If not used, leave
24	PCM_OUT	DO	PCM data output	If not used, leave
25	RESERVE	OD	Reserved	If not used, leave
26	IRIG_B	DO	B code time synchronization	If not used, leave
27	GND	G	GND	
28	PCM_SYN	DIO	PCM synchronous clock	If not used, leave
29	NC			
30	USIM0_R	DO	Reset (U)SIM1 card.	If not used, leave
31	NC			
32	USIM0_CL	DO	(U)SIM1 card clock	If not used, leave
33	GND	G		
34	USIM0_D	DIO	SIM1 card data	If not used, leave
35	NC			
36	USIM0_P	PO	(U)SIM1 card power supply	If not used, leave
37	NC			
38	WAKE_IN	DI	Wake up the module.	
39	GND	G	GND	
40	USIM1_D	DI	Detection of USIM2 card	If not used, leave
41	PETn0	AO	PCIe transmission (-)	If not used, leave
42	USIM1_D	DIO	(U)SIM2 card data	If not used, leave
43	PETp0	AO	PCIe transmit (+)	If not used, leave
44	USIM1_CL	DO	SIM2 card clock	If not used, leave
45	GND	G	GND	
46	USIM1_R	DO	Reset (U)SIM2 card.	If not used, leave
47	PERn0	AI	PCIe receive (-)	If not used, leave
48	USIM1_P	PO	(U)SIM2 card power supply	If not used, leave
49	PERp0	AI	PCI Express receive (+)	If not used, leave
50	PERST#	OD	PCIe reset	If not used, leave
51	GND	G	GND	
52	CLKREQ#	OD	PCIe clock request	If not used, leave
53	REFCLKN	AIO	PCIe reference clock (-)	If not used, leave
54	PEWAKE	OD	PCIe wake-up	If not used, leave
55	REFCLKP	AIO	PCIe reference clock (+)	If not used, leave
56	ANT_CTR	DO	RF antenna switch control	If not used, leave
57	GND	G	GND	
58	ANT_CTR	DO	RF antenna switch control	If not used, leave

Pin number	Pin names	Type	Description	Note
59	NC			If not used, leave
60	I2C_SCL	OD	I2C Clock	If not used, leave
61	NC			If not used, leave
62	UART_RX	DI	Main serial port reception	If not used, leave
63	PPS_OUT	DO	Pulse per second	If not used, leave
64	UART_TX	DO	Main serial port transmission	If not used, leave
65	VDD_EXT	PO	Module 1.8V output	If not used, leave
66	USIM0_D	DI	Detection of SIM1 card	If not used, leave
67	RESET#	DI	Module reset	If not used, leave
68	I2C_SDA	OD	I2C data	If not used, leave
69	CONFIG_1	DO	The voltage value is determined by the host end for M.2 port type identification.	If not used, leave floating
70	VBAT	PI	Module main power supply	
71	GND	G	GND	
72	VBAT	PI	Module main power supply	
73	GND	G	GND	
74	VBAT	PI	Module main power supply	
75	CONFIG_2	DO	The voltage value is determined by the host end for M.2 port type identification.	If not used, leave floating

2.6 Assessment Suite

Lierda can provide a complete evaluation and development kit, including an ADP board for easy debugging of the minimum system, an EVB board containing peripherals such as audio, WIFI, and other accessories, making development convenient.

3 Nature of work

3.1 Work Mode

Table 3-1 NR90-HCN M.2 Module Operating Modes Description

Working mode	Function	
Normal working mode	IDLE	The software is running normally. The module is registered on the network and able to receive and send data.
	Talk /Data	The network connection is working properly. In this mode, the module's power consumption depends on the network settings and data transmission rate.
Minimum Function Mode	When the power supply is uninterrupted, using AT+CFUN=0 can set the module to minimum functionality mode. In this mode, the RF does not work.	
Airplane mode	AT+CFUN=4 or pulling down the W_DISABLE# pin can set the module to flight mode. In this mode, the RF does not work.	
Sleep mode	In this mode, the module's power consumption will be reduced to a very low level, but the module can still receive paging, SMS, calls, and TCP/UDP data.	
Shutdown mode	In this mode, the PMU stops supplying power to the baseband and RF sections, the software stops working, and the serial port is not accessible.	

3.2 Hibernate mode

In sleep mode, the DRX function of the module can reduce the module's power consumption and broadcast the DRX index cycle value through the wireless network. The following figure shows the relationship between the DRX operating time and the current consumption in sleep mode of the module. The longer the DRX cycle, the lower the power consumption.

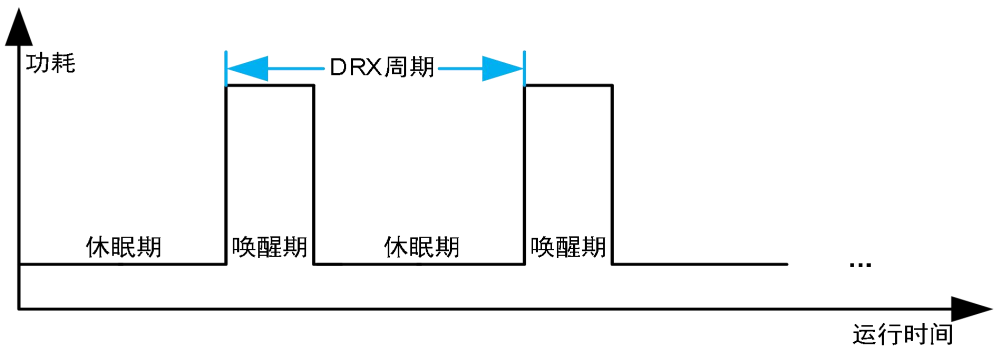


Figure 3.1 Relationship between DRX operation time and power consumption in sleep mode.

The process of entering and exiting sleep mode for the NR90-HCN M.2 module is as follows:

- When the module is in the wake-up state, the host pulls down the WAKE_IN pin through a GPIO, and this GPIO can remain at a low level during sleep.
- The module is in sleep mode, and the host pulls up the WAKE_IN pin through a GPIO, and this GPIO can maintain a high level continuously in the wake-up state.

The reference design of the WAKE_IN interface is as follows.

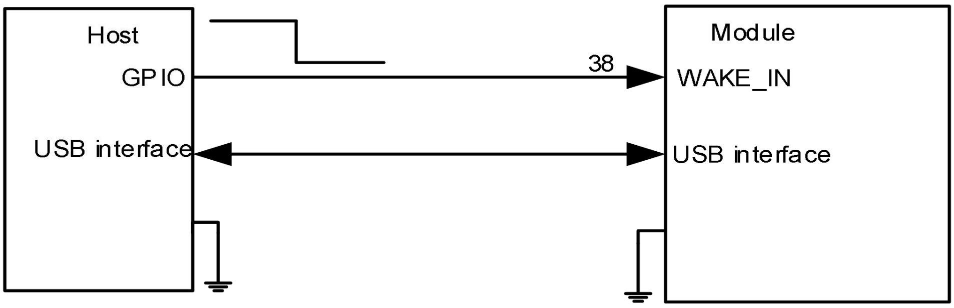


Figure 3.2 WAKE_IN Interface Reference Design Circuit

The host can pull up WAKE_IN through a GPIO to wake the module up from sleep mode.

3.3 Power supply design

Table 3-2 Power Supply Pin Definitions

Pin number	Type	Pin names	Description	Minimum value	Typical value	Maximum value	Unit
2, 4, 70, 72, 74	PI	VBAT	Module main power supply	3.3	3.8	4.4	V
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	G	GND	GND				

To ensure the normal operation of the NR90-HCN M.2 module, the system power supply VBAT needs to be maintained within the range of 3.3V-4.4V (typical value 3.8V).

When the module is used with different external devices, attention should be paid to the power supply design of the module. In any case, it is necessary to ensure that the module power supply voltage is maintained above 3.3V, otherwise the module will not be able to operate normally.

External power supply LDO or DCDC selection advice: The selected component should be able to provide a current of 3A or more, and at least 2 220uF energy storage capacitors should be connected in parallel on VBAT. In addition, to reduce the impact of PCB traces on the power supply voltage, VBAT traces should be kept as short and wide as possible, with a width of no less than 2mm. To improve the stability of the power supply, it is recommended to add a voltage-regulating diode near the VBAT pin of the module with a power dissipation greater than 0.5W and a reverse voltage of 5.1V. The reference circuit is shown in the diagram below.

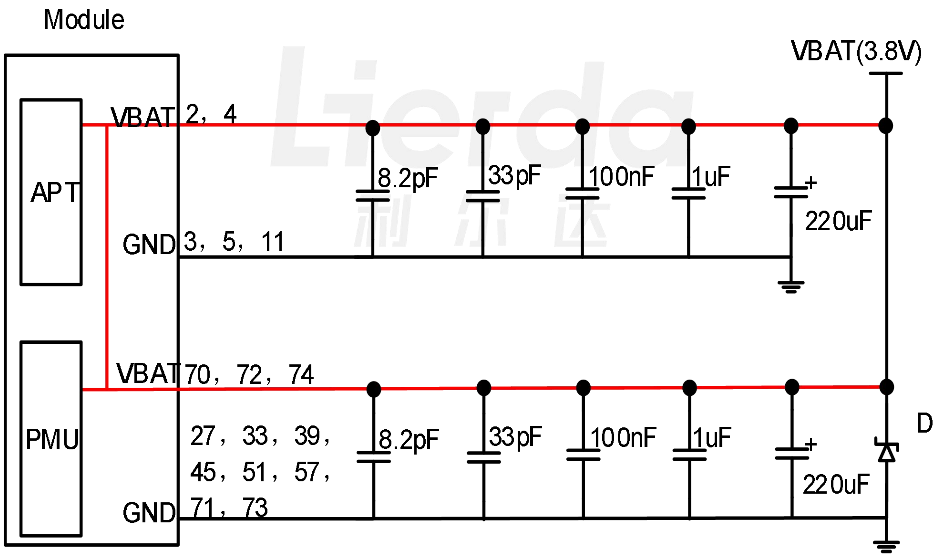


Figure 3.3 Power Supply Recommended Design

Table 3-3 Description of Capacitor Applications

Recommend capacitors	Application	Explanation
220uF×2	Stabilizing tantalum capacitor	Reduce power fluctuations during module operation, requiring the use of low ESR capacitors. (1) The power supply requirement for LDO or DCDC should not be

		less than 440uF capacitance. (2) The battery power supply can be appropriately reduced to 100-220uF capacitance.
1uF，100nF	Digital signal noise	Filter out interference generated by clock and digital signals.
33pF	700, 850/900MHz frequency band	Filter out low-frequency RF interference.
8.2pF	1700/1800/1900, 2100/2300, 2500/2600MHz frequency bands	Filter out RF interference in the mid/high frequency bands.

3.4 Power on/off

The NR90-HCN M.2 module achieves power on/off function through the POWER_ON_OFF# pin.

Table 3-4 POWER_ON_OFF# Interface Description

Pin numb	Pin names	Type	Description	Parameter	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
6	POWER_ON_OFF#	DI	Module power on/off control	VIH	1.2	1.8	4.4	High level to power on, low level to power off, pulled down to GND inside the
				VIL	-	-	0.2	

3.4.1 Power on.

When the NR90-HCN M.2 module is in the powered-off state, the module can be turned on by applying a high-level signal to the POWER_ON_OFF# pin, which can be a 1.8V or 3.3V GPIO signal. Internally, this pin on the module is pulled down to GND through a 100K resistor, so the module is initially powered off by default when powered on.

The host powers on by pulling the POWER_ON_OFF# pin high through GPIO, the reference circuit is shown below.

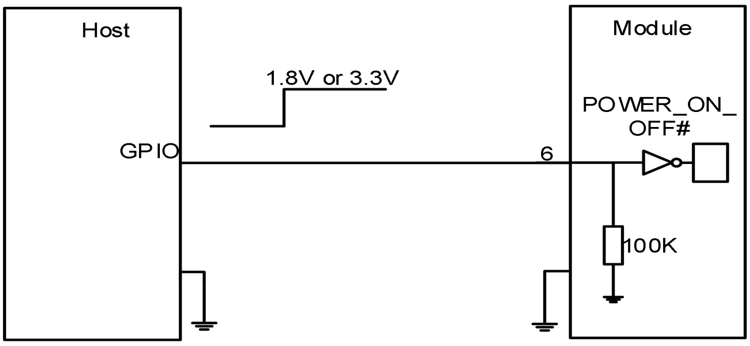


Figure 3.4 GPIO control module boot-up.

The power-on sequence is as shown in the following figure.

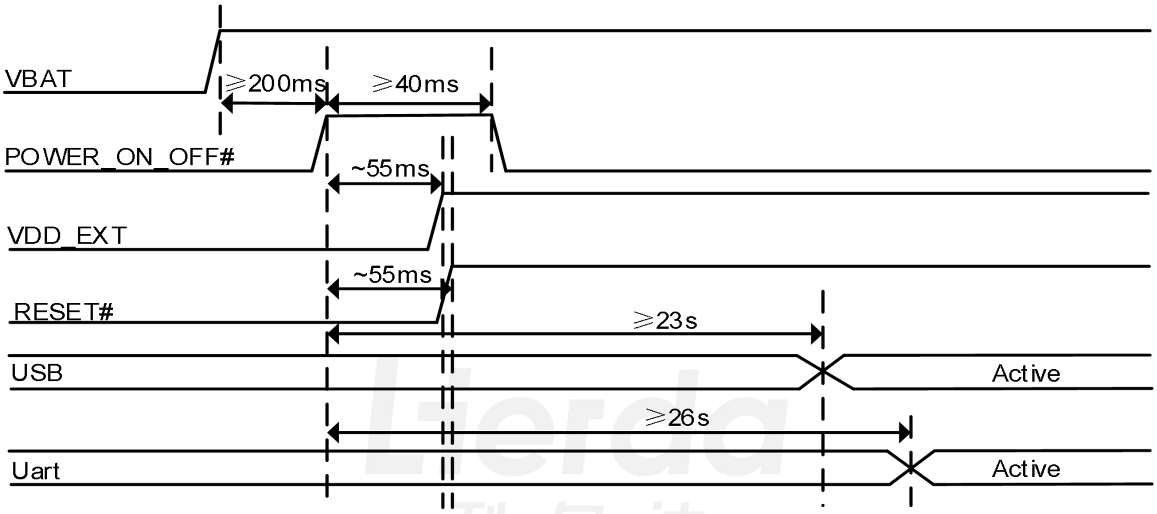


Figure 3.5 Power-on Timing Diagram

Note

Before pulling up the POWER_ON_OFF# pin, ensure that the VBAT voltage is stable. It is recommended to have a time interval of no less than 200 ms between applying power to VBAT and pulling up the POWER_ON_OFF# pin. The timing here is related to the business of powering on UART and USB. In terms of the time for AT commands, the difference in time between the two is not significant.

3.4.2 Shutdown

When the module is in the power-on state, the host pulls down the POWER_ON_OFF# pin through GPIO, and the module will execute the shutdown process. The following diagram shows the shutdown principle of the module. Additionally, shutdown can also be performed using the AT+LPOWD command.

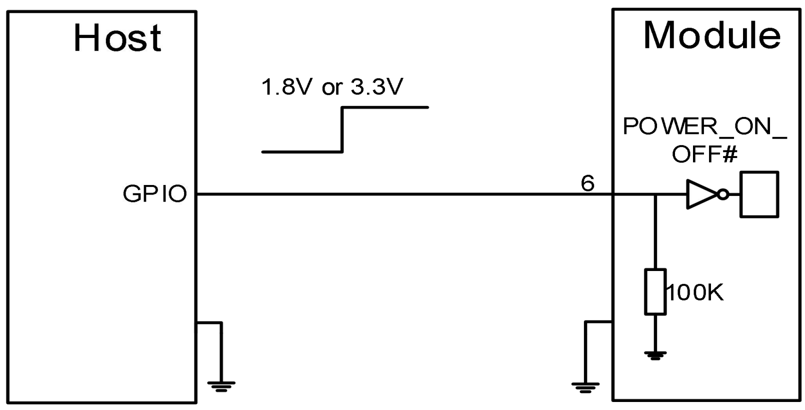


Figure 3.6 GPIO control module shutdown

Shutdown timing diagram is as shown below:

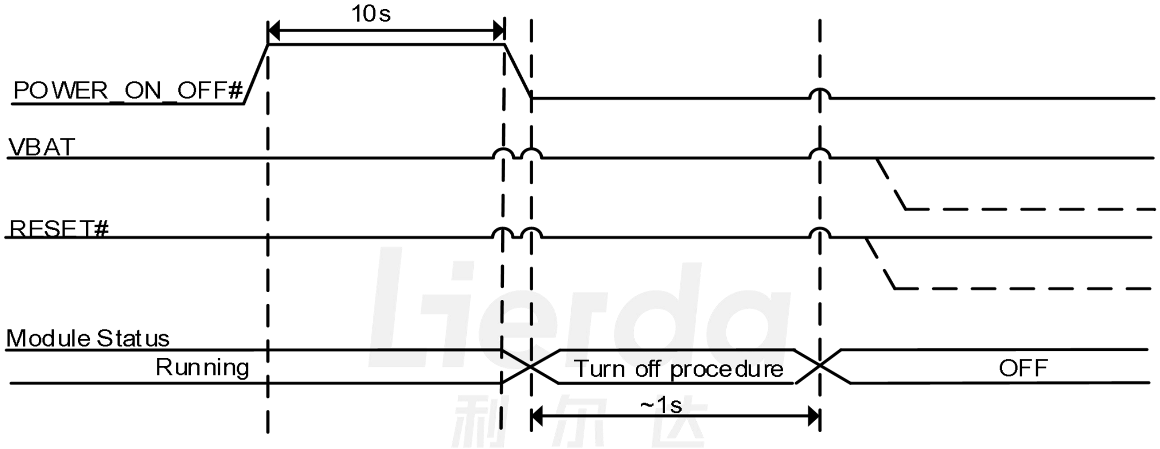


Figure 3.7 Shutdown Timing Diagram

Note

When the module is working normally, do not cut off the power supply immediately to avoid damaging the Flash inside the module. It is recommended to first turn off the module using POWER_ON_OFF# or AT+LPOWD, and then disconnect the power supply.

After the AT command is executed successfully, it will return OK. Then the UE activates the network and outputs POWERED DOWN to enter the shutdown state. The maximum duration for network activation is 60 seconds, and the customer should pay attention to the shutdown time in the design. To avoid data loss, the module must not be powered off before outputting POWERED DOWN.

3.5 Reset

The NR90-HCN M.2 module can be reset by using the RESET# pin.

Table 3-5 RESET# Interface Description

Pin number	Pin name	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
67	RESET#	DI	Module reset	VIH	1.17	1.8	1.98	
				VIL	-0.3	-	0.63	

When the module software stops responding, pull down the RESET# pin for 250ms or longer. The RESET# signal is sensitive to interference, so it is recommended to keep the traces on the module interface board as short as possible and have proper GND handling.

Customers can use an open-drain drive circuit or a button to control the RESET# pin, refer to the circuit as shown in the following diagram.

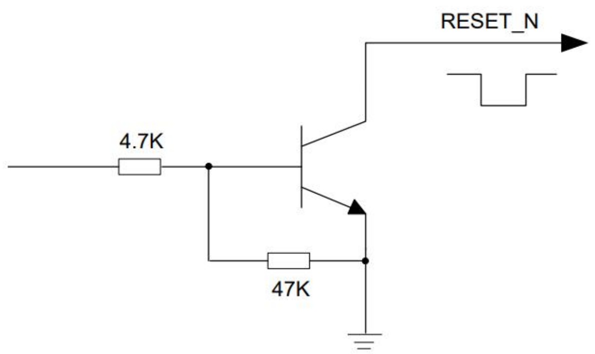


Figure 3-8 Open-Drain Driven Reset Reference Circuit

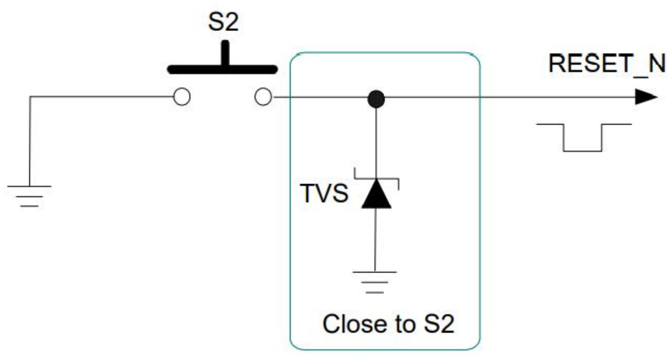


Figure 3.9 Key Reset Reference Circuit

The reset timing diagram is as follows:

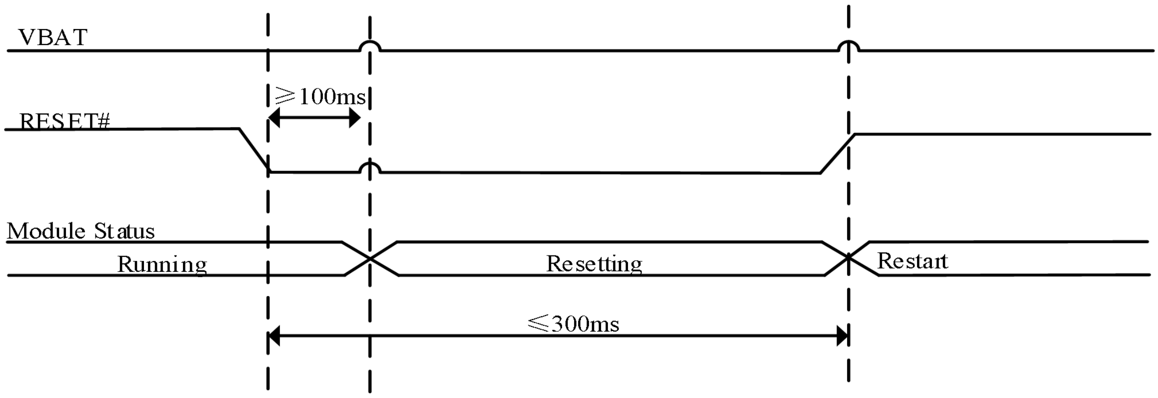


Figure 3.10 RESET# Timing Diagram

Note

- Ensure that the maximum load capacitance for the POWER_ON_OFF# and RESET# pins does not exceed 47pF.
- The reset function should only be used after the AT+LPOWD command and POWER_ON_OFF# shutdown fail.

4 Application Interface

The physical interface and electrical characteristics of the NR90-HCN M.2 module comply with the PCI Express M.2 Specification. This chapter mainly introduces the definition of the interface and its related applications.

- UART interface
- USB interface
- PCIe interface
- (U)SIM interface
- I2C interface
- PCM interface
- Control and status indicator interface
- Time synchronization interface
- ANT_CTRL interface*
- Configure pins
- Antenna interface

4.1 UART interface

The NR90-HCN M.2 module has one serial port, which can be used for AT command sending and data transmission, with a default baud rate of 115200bps.

Table 4-1 UART Interface Pin Description

Pin	Pin	Ty	Description	Param	Minimum	Typical	Maximu	Note
62	UART_RXD	DI	Main serial port reception	VIH	1.17	1.8	1.98	If not used, leave floating
				VIL	-0.3	-	0.63	
64	UART_TXD	DO	Main serial port transmission	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	

When using the serial port interface, pay attention to the issue of level consistency.

(1) Transistor level conversion reference circuit

This circuit does not have special requirements for the power supply voltage of the module, and it is low cost, but there are restrictions on the serial port baud rate. Please refer to the design below, and pay attention to the direction of level conversion.

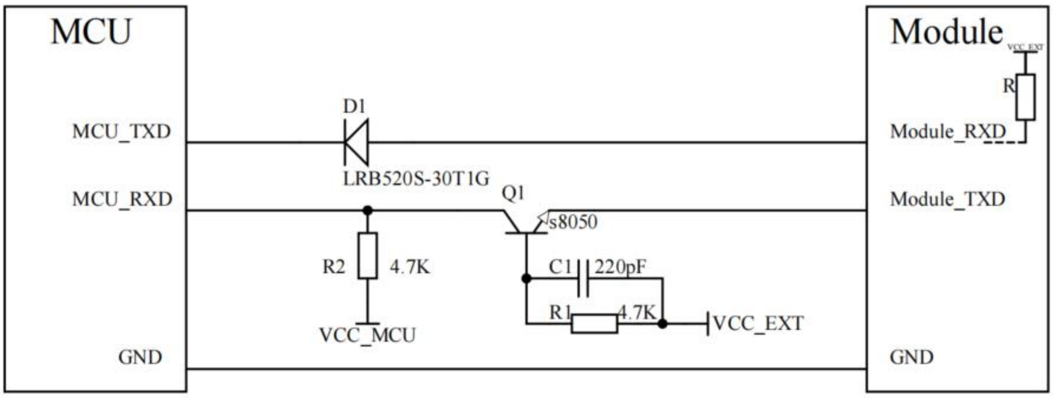


Figure 4.1 Transistor Level Conversion Reference Circuit

Note

- If the module has no internal pull-up, the diode conversion circuit requires an external pull-up from the user, NR90-HCN M.2 internally pulls up through a 20K resistor to a 1.8V voltage domain.
- In this circuit, MCU_TXD defaults to outputting 3.3V, and VCC_EXT defaults to 1.8V. For the diode conversion circuit, it should be noted that the cathode voltage of the diode needs to be higher than the anode voltage in order to achieve the function of the circuit mentioned above.
- This level conversion circuit is not suitable for applications with a baud rate exceeding 460Kbps.

(2) MOSFET level conversion reference circuit

This circuit has no special requirements for the power supply voltage of the module, and it is low cost, able to meet the requirement of serial port baud rate 921600bps. The reference design is as follows, pay attention to the direction of level conversion.

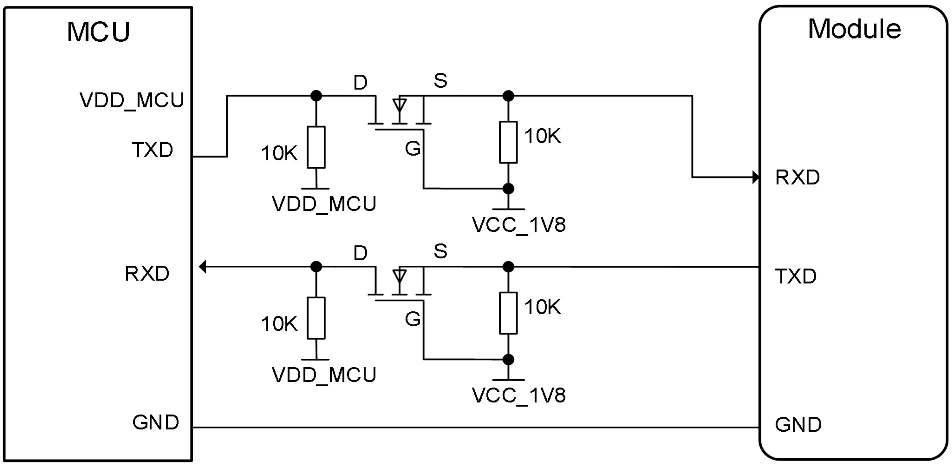


Figure 4.2 MOSFET Level Conversion Reference Circuit

Recommend MOSFET for reference:

Brand: LRC; Specification Model: L2N7002LT1G, the corresponding internal principle is as follows:

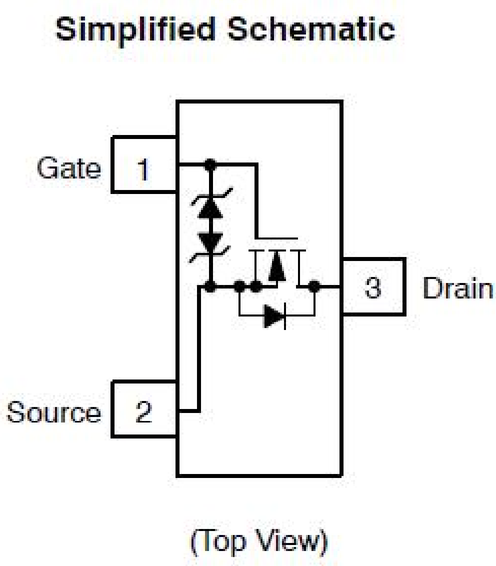


Figure 4.3 MOSFET device diagram

4.2 USB interface

The NR90-HCN M.2 module complies with the USB 2.0 specification. When acting as a host, it supports HS (480Mbps)/FS (12Mbps)/LS (1.5Mbps), and when acting as a device, it supports HS (480Mbps)/FS (12Mbps). The USB interface can be used for AT command transmission, data transfer, software debugging, and firmware upgrades. The table below shows the pin definitions of the USB interface.

Table 4-2 USB Interface Pin Description

Pin number	Pin names	Type	Describe	Note
7	USB_DP	AIO	USB 2.0 differential data (+)	90Ω differential impedance
9	USB_DM	AIO	USB 2.0 differential data (-)	

It is recommended that the customer design to reserve the USB 2.0 interface for firmware upgrade while also reserving test points. Please refer to the design circuit below:

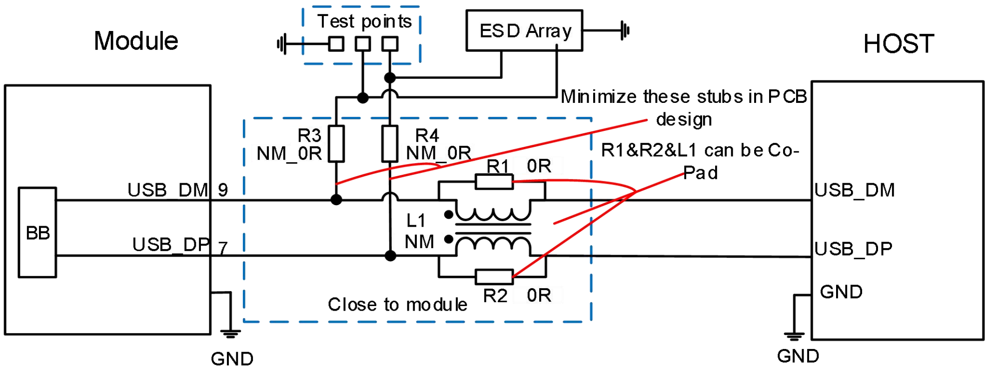


Figure 4.4 USB reference design diagram

Note

- It is recommended to connect a common mode inductor L1 between the host and the module to prevent USB signal EMI interference. Alternatively, a 0Ω resistor can be used for direct connection, designed to share the same pad with L1. Depending on the debugging situation, either a common mode inductor or a resistor can be used. Additionally, it is suggested to connect resistors R3 and R4 to test points for debugging purposes, with the resistors not populated by default. To meet the USB data line signal integrity requirements, L1, R1, R2, R3, and R4 should be placed close to the module, with R3 and R4 placed close to each other. The routing of the lines connecting the test points should be kept as short as possible.
- In the circuit design of the USB interface, to ensure the performance of USB, the following principles are recommended to be followed in the circuit design: Ground processing is needed around the USB routing, using 90Ω differential impedance lines. Do not route USB lines under crystal oscillators, oscillators, magnetic devices, DC-DC power

inductors, and RF signals. It is recommended to use inner-layer differential lines, and surround them with ground on all sides. When selecting ESD protection devices on the USB data lines, attention should be paid to ensuring that the parasitic capacitance of USB 2.0 does not exceed 1pF, placing the ESD protection device as close to the USB interface as possible, and ensuring that the signal passes through the ESD protection device first.

4.3 PCIe interface

The NR90-HCN M.2 module contains a PCIe interface that complies with the PCIe 2.0 specification. The main features are as follows:

- Support PCIe 1.1
- The working speed is 2.5Gbit/s (Gen1).
- RC mode only

Table 4-3 PCIe Interface Pin Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
41	PETn0	AO	PCIe transmits data (-)					
43	PETp0	AO	PCIe data transmission (+)					
47	PERn0	AI	PCIe receive data (-)					
49	PERp0	AI	PCIe receive data (+)					
53	REFCLKN	AIO	PCIE reference clock (-)					
55	REFCLKP	AIO	PCIe reference clock (+)					
50	PERST#	OD	PCIe reset	The leakage pole opens the way, and the voltage value is determined by the host				
52	CLKREQ#	OD	PCIe clock request	The leakage pole opens the way, and the voltage value is determined by the host				
54	PEWAKE	OD	PCIe Wakeup	The leakage pole opens the way, and the voltage value is determined by the host				

The following diagram is the reference circuit of NR90-HCN M.2 connecting PCIe device using PCIe interface:

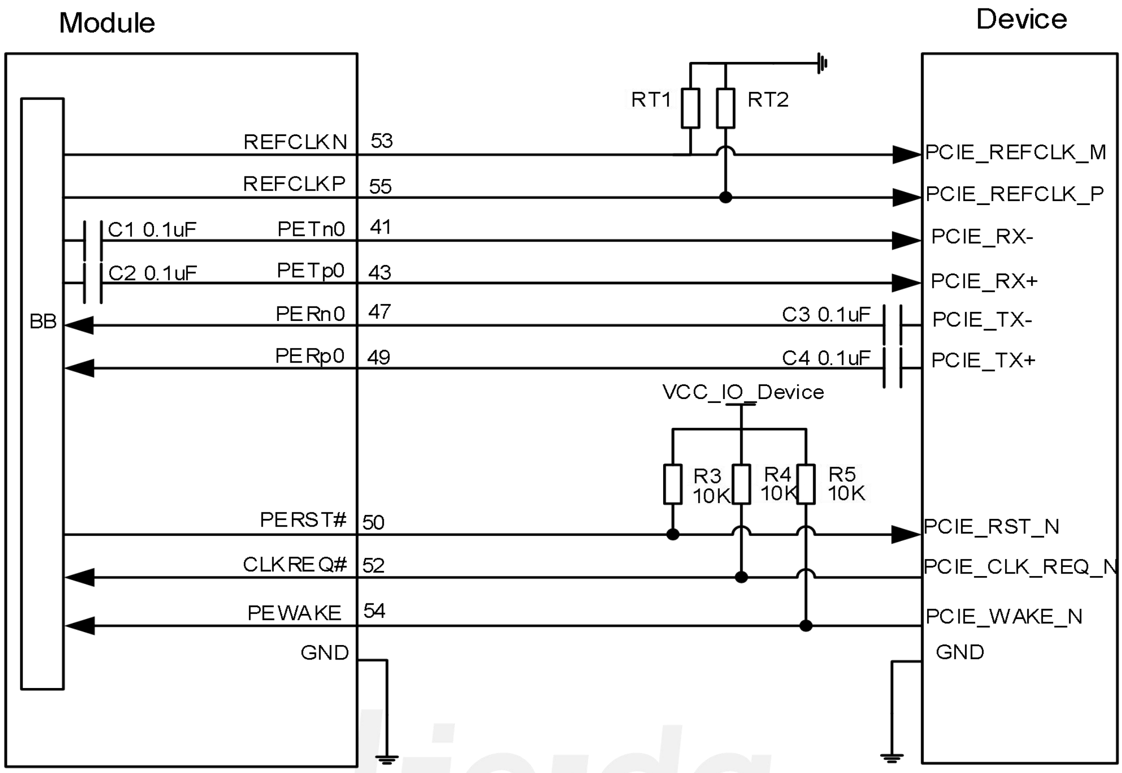


Figure 4.5 Reference Design for Module Connection to PCIe Device

Note

- C3 and C4, the decoupling capacitors, should be placed close to the Tx PIN. It is recommended to use 0.1uF, +/-10%, X5R or X7R capacitors. C1 and C2 have been integrated into the module internally, so there is no need to add these two capacitors when designing the terminal equipment.
- RT1 and RT2 two terminal resistors are in use, please consult our FAE.
- CLK, TX, and RX differential signal lines need to be routed to control the differential impedance at 100Ω +/-10%.
- When routing PCIe, it should stay away from sensitive signal sources such as RF, audio, and crystal oscillators.
- PCIe traces cannot be routed under components and must not cross paths with other signals.

- CLK, TX, and RX should be routed in differential pairs, ensuring top, bottom, left, right, and three-dimensional grounding.
- M.2 interface devices do not support hot-swapping of PCIe devices, requiring a restart after reinsertion.

4.4 (U)SIM card interface

(U)The SIM card interface complies with ETSI and IMT-2000 card specifications, supporting 1.8V and 3.0V (U)SIM cards, and also supports dual SIM dual standby function. The table below describes the interface definition of (U)SIM.

Table 4-4 (U)SIM Card Interface Definition

Pin	Pin	Typ	Descriptio	Para	Minimum	Typical	Maximum	Note
30	USIM0_RESET	DO	Reset (U)SIM1 card	VOH	1.4/2.25	1.8/3.0	2.0/3.3	If not used, leave floating
				VOL	-	-	0.45/0.375	
32	USIM0_CLK	DO	SIM1 card clock	VOH	1.4/2.25	1.8/3.0	2.0/3.3	If not used, leave floating
				VOL	-	-	0.45/0.375	
34	USIM0_DATA	DIO	SIM1 card data	VIH	1.27/1.875	1.8/3.0	1.98/3.3	If not used, leave floating
				VIL	-0.3	-	0.58/0.75	
				VOH	1.4/2.25	1.8/3.0	2.0/3.3	
				VOL	-	-	0.45/0.375	
36	USIM0_PWR	PO	SIM1 card power	-	1.62	1.8/3.0	3.3	If not used, leave floating
66	USIM0_DETECT	DI	Detection of SIM1 card	VIH	1.17	1.8	1.98	Pay attention to logic insertion, software and hardware design should be consistent.
				VIL	-0.3	-	0.63	
40	USIM1_DET	DI	Detection of SIM2 card	VIH	1.17	1.8	1.98	
				VIL	-0.3	-	0.63	
42	USIM1_DATA	DIO	(U)SIM2 card data	VIH	1.27/1.875	1.8/3.0	1.98/3.3	If not used, leave floating
				VIL	-0.3	-	0.58/0.75	
				VOH	1.4/2.25	1.8/3.0	2.0/3.3	
				VOL	-	-	0.45/0.375	

44	USIM1_CLK	DO	(U)SIM2 card clock	VOH	1.4/2.25	1.8/3.0	2.0/3.3	If not used, leave floating
				VOL	-	-	0.45/0.375	
46	USIM1_RST	DO	Reset (U)SIM2 card	VOH	1.4/2.25	1.8/3.0	2.0/3.3	If not used, leave floating
				VOL	-	-	0.45/0.375	
48	USIM1_PWR	PO	(U)SIM2 card power	-	1.62	1.8/3.0	3.3	If not used, leave floating

The schematic diagram of the (U)SIM interface circuit design is as follows:

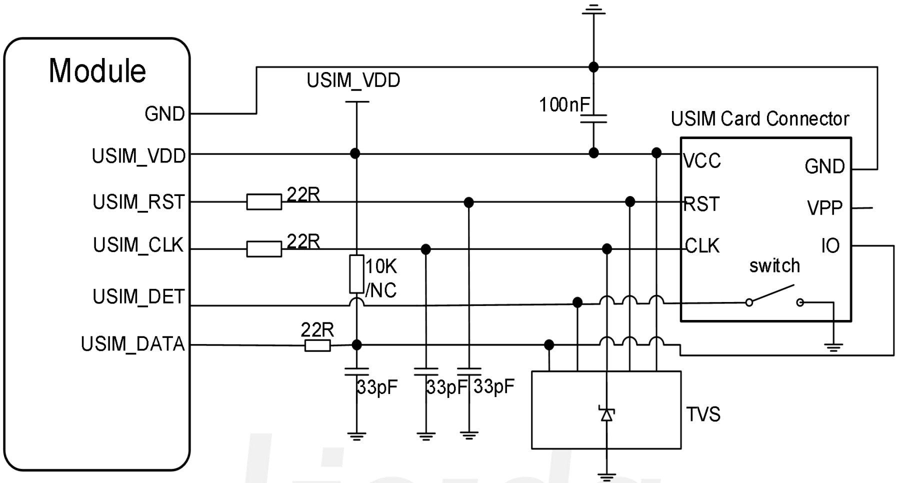


Figure 4.6 8-pin (U)SIM interface reference circuit diagram

The principle explanation of the SIM card slot with detection signal is as follows (when designing the principle, pay attention to the logic of card insertion). Taking the MUP-C792 card slot connector as an example, the specification sheet describes the Detect Switch as follows,

ELECTRIC FUNCTION	DETECT SWITCH
WITHOUT CARD	CLOSED
CARD INSERTED	OPEN

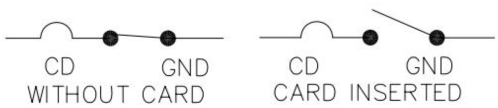


Figure 4.7 SIM card connector Detect Switch operation block diagram

Therefore,

- When the SIM card is inserted, USIM_DET is at a high level.
- When the SIM card is removed, USIM_DET is at a low level.

If the USIM card detection function is not needed, please leave the USIM_DET pin floating. The following is the 6-pin USIM interface reference circuit:

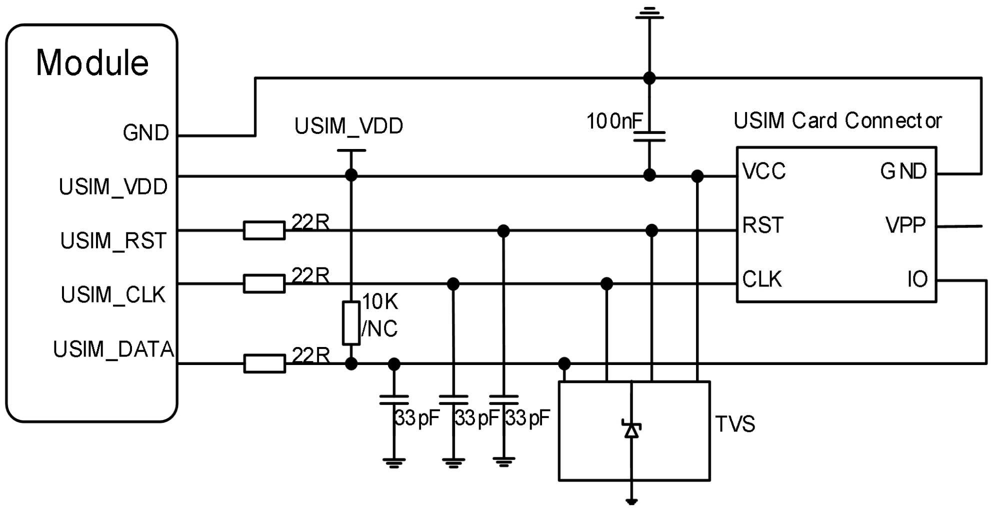


Figure 4.8 6-pin (U)SIM interface reference circuit diagram

4.4.1 Hot-swappable (U)SIM

The NR90-HCN M.2 module supports (U)SIM card hot-plugging function, determines the insertion and removal of (U)SIM card by detecting the USIM_DET pin status of the (U)SIM card slot, thus supporting (U)SIM card hot-plugging function. The (U)SIM card hot-plugging function can be configured using the AT+LSIMDET command.

This command is used to query/enable/disable the card detection of the (U)SIM card. GPIO interrupt is used for (U)SIM card detection, and the detection pin level needs to be set when inserting the (U)SIM card.

Test command AT+LSIMDET=?	Response +LSIMDET: (Supported <enable> list), (Supported <insert_level>) List OK
Query command AT+LSIMDET?	Response +LSIMDET:<enable>,<insert_level> OK
Set command	Response

AT+LSIMDET=<enable>,<insert_level>	OK Or ERROR
Maximum response time	3 seconds
Feature Description	The command will take effect after a restart; Automatic save after parameter configuration.

Parameters

Integer type. Enable/disable (U)SIM card detection function.

0 Disable

1 Enable

`<insert_level>` is an integer. Detect the level of the pins when inserting the (U)SIM card.

0 Low Level

1 High Level

Table 4-5 USIM_DET Control Voltage Description

AT format	AT command	SIM card hot swap detection	Function Description
Read Command AT+QSIMSTAT? Write Command AT+QSIMSTAT=<enable>,<insert_level>	AT+LSIMDET=1,0	Start	The (U)SIM card hot-plug detection function is enabled, and the module detects whether the (U)SIM card is inserted through the USIM_DET pin status detection, low-level detection.
	AT+LSIMDET=1,1	Start	The hot-plug detection function of the (U)SIM card is enabled, and the module detects whether the (U)SIM card is inserted through the USIM_DET pin status detection, detecting a high level.
	AT+LSIMDET=0,	Close	SIM card hot swap detection function disabled, module reads (U)SIM card during startup, does not detect USIM_DET status

	0 AT+LSIMDET=0,1		

Note

- NR90-HCN M.2 module (U)SIM card hot swap function is disabled by default.
- If hot swap is enabled, the <insert_level> value must match the hardware-designed insertion level, otherwise the hot swap function will be invalid.
- If a (U)SIM card has been successfully detected, the command to control the (U)SIM card detection function is no longer supported. The command to control (U)SIM card detection function can only be used after the module is restarted or the (U)SIM card is hot-swapped.

4.4.2 Requirements for (U)SIM card interface design

In the circuit design of the (U)SIM card interface, in order to ensure the good functional performance of the (U)SIM card and prevent damage, the following design principles are recommended to be followed in the circuit design:

- The distance between the (U)SIM card slot and the module holder should not be too far apart, the closer the better, try to ensure that the (U)SIM card signal line wiring does not exceed 200mm.
- (U)SIM card signal line wiring should be kept away from RF lines and VBAT power lines.
- To prevent possible crosstalk from the USIM_CLK signal to the USIM_DATA signal, the wiring of the two should not be too close. Ground shielding should be added between the two traces, and ground protection is also required for the USIM_RST signal.
- To ensure good ESD protection, it is recommended to add TVS diodes placed near the (U)SIM card holder. The parasitic capacitance of the selected ESD device should not exceed 10pF. A 0-ohm resistor can also be placed in series between the module and the

(U)SIM card for debugging purposes. 33pF capacitors should be connected in parallel on the USIM_DATA, USIM_CLK, and USIM_RST lines to filter out RF interference. Peripheral components of the (U)SIM card holder should be placed as close as possible to the (U)SIM card holder.

- The pull-up resistor of the USIM_DATA is beneficial for increasing the anti-interference ability of the (U)SIM card. It is recommended to reserve a pull-up resistor near the (U)SIM card slot when the (U)SIM card traces are too long or in close proximity to the interference source.

4.5 I2C Interface

The NR90-HCN M.2 module provides a set of I2C interfaces, supporting standard mode and fast mode.

Table 4-6 I2C Interface Description

Pin	Pin	Ty	Descripti	Param	Minimum	Typical	Maximum	Note
60	I2C_SCL	OD	I2C clock signal	VIH	1.17	1.8	1.98	If not used, leave floating
				VIL	-0.3	-	0.63	
				VOH	1.35	1.8	1.98	
				VOL	-0.3	-	0.45	
68	I2C_SDA	OD	I2C data signal	VIH	1.17	1.8	1.98	If not used, leave floating
				VIL	-0.3	-	0.63	
				VOH	1.35	1.8	1.98	
				VOL	-0.3	-	0.45	

The I2C interface schematic diagram is as shown in the figure below, pay attention to level matching when designing the principle:

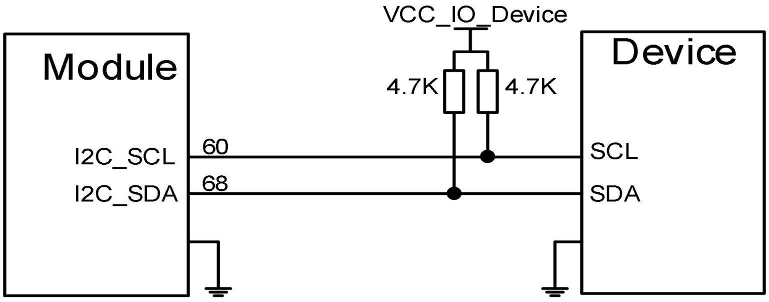


Figure 4.9 I2C Reference Design

Note

Pull-up resistors on the I2C bus can be adjusted based on actual test results.

4.6 PCM interface

The NR90-HCN M.2 module supports external connection to CODEC via PCM interface.

Table 4-7 PCM Interface Description

Pin	Pin	Ty	Description	Param	Minimum	Typical	Maximum	Note
22	PCM_IN	DI	PCM data input	VIH	1.17	1.8	1.98	If not used, leave floating
				VIL	-0.3	-	0.63	
24	PCM_OUT	DO	PCM data output	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	
28	PCM_SYNC	DO	PCM synchronous output	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	
20	PCM_CLK	DO	PCM clock output	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	

External CODEC device schematic diagram is as shown in the following figure:

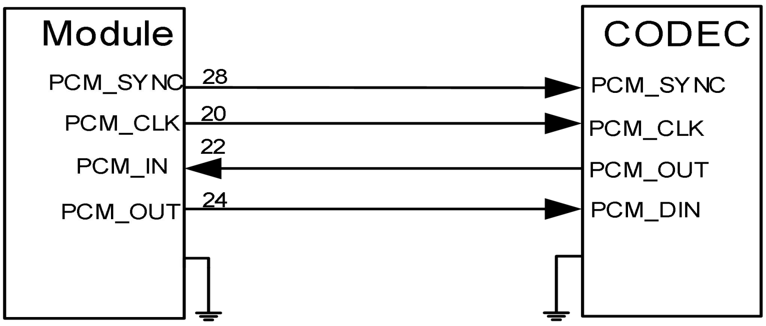


Figure 4.10 PCM Reference Design

4.7 Control and status indicator interface

4.7.1 Status indicator LED

The NR90-HCN M.2 module drives the LED through the LED1# pin, which allows a maximum input current of 20mA.

Table 4-8 LED1# Interface Description

Pin number	Pin Names	Type	Description	Parameters	Note
10	LED1#	OD	Module status indicator LED	Maximum sink current 20mA	

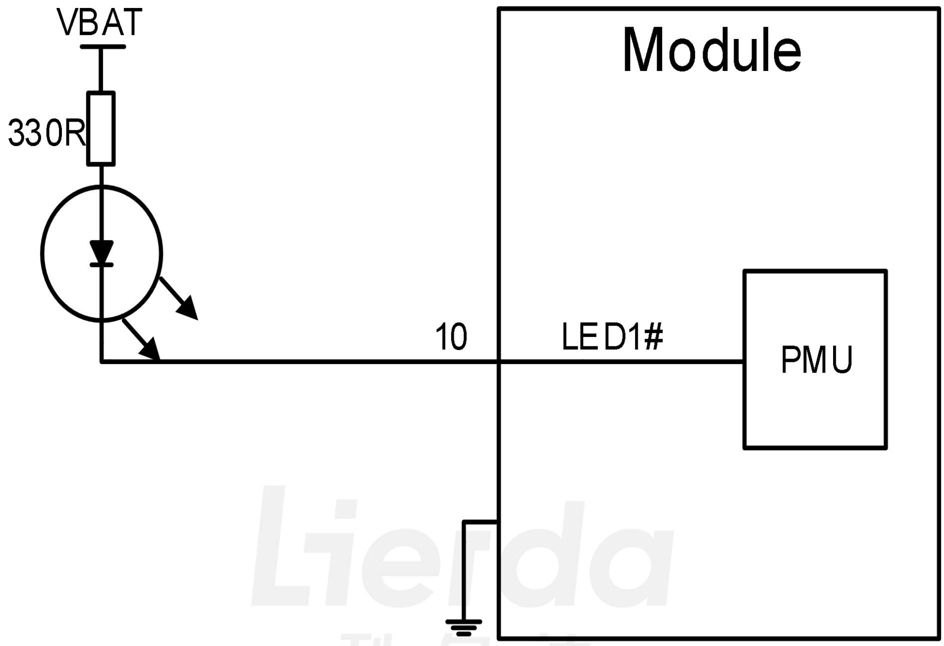


Figure 4.11 Reference circuit for the module status indicator interface of the NR90-HCN M.2 module.

4.7.2 Flight mode

The NR90-HCN M.2 module controls the activation or deactivation of the flight mode through the W_DISABLE# pin. This pin is compatible with two voltage domains, 1.8V and 3.3V. In addition to this method, the flight mode can also be activated or deactivated through AT commands.

Table 4-9 NR90-HCN M.2 W_DISABLE# Pin Description

Pin number	Pin names	Type	Description	Parameters	Note
8	W_DISABLE#	DI	Module flight mode control	Compatible with 1.8V and 3.3V voltage domains.	If not used, leave floating

Table 4-10 NR90-HCN M.2 module supports two ways to enter flight mode.

Serial number	Control method	Control operation
1	Hardware I/O interface button control	Pull up or suspend (default to pull up) W_DISABLE# for normal mode, pull down for flight mode.
2	AT command control	AT+CFUN=4--Enter flight mode AT+CFUN=0--Minimum Function Mode (turn off RF and SIM card) AT+CFUN=1--Full functionality mode

The reference design of the W_DISABLE# interface is shown in the figure below, where the typical value of VCC_IO_HOST can be 1.8V or 3.3V.

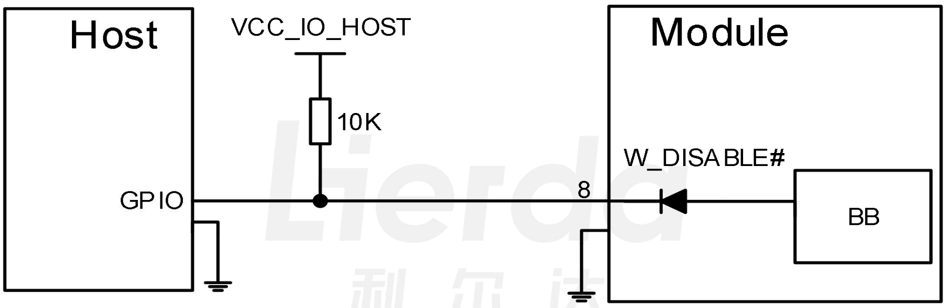


Figure 4.12 Reference Circuit for the W_DISABLE# Interface of the NR90-HCN M.2 Module

4.7.3 Wake up the host.

NR90-HCN M.2 module wakes up the host through the WOWWAN# pin. This pin is an open-drain form output signal, so a pull-up resistor needs to be added at the host end.

Table 4-11 NR90-HCN M.2 Wake Host Interface Description

Pin number	Pin names	Type	Description	Parameters	Note
23	WOWWAN#	OD	Wake up the host	Low level effective	If not used, leave floating

Table 4-12 NR90-HCN M.2 Signal Status

Pin status	Module running status
Output a low-level pulse signal of 1s.	Phone/short message/data incoming (wake up the host)
Always at a high level.	Idle state/sleep mode

The interface reference design of WOWWAN# is as shown in the figure below. Since this pin is an open-drain, the voltage value of VCC_IO_HOST is determined by the host side.

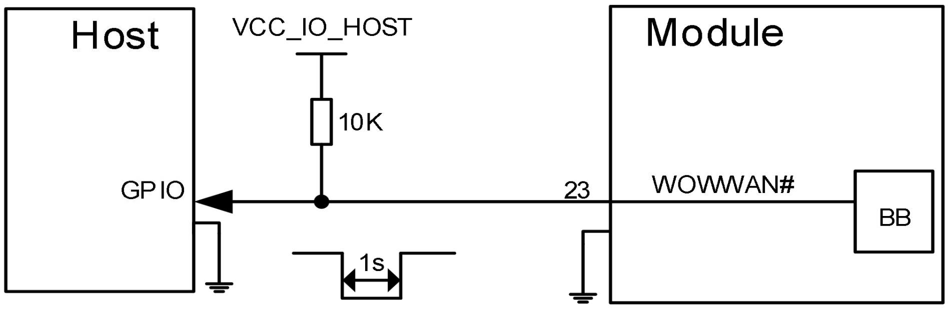


Figure 4.13 WOWWAN# Interface Reference Circuit

4.8 Time synchronization interface

The NR90-HCN M.2 module provides two timing interfaces for external devices. They are B-Code and 1PPS output respectively.

Table 4-13 NR90-HCN M.2 Timing Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
26	IRIG_B	DO	B code output	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	
63	PPS_OUT	DO	1PPS output	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	

The following is the reference circuit of the B-code output interface:

Figure 4.14 B-code output interface reference circuit

The following is the reference circuit for the 1PPS output interface:

Figure 4.15 1PPS Output Interface Reference Circuit

4.9 Pin configuration

The NR90-HCN M.2 module has four configuration pins, defined as in the following table.

Table 4-14 NR90-HCN M.2 Module Configuration Pin Description

Pin numb	Pin names	Type	Description	Parameters	Note
21	CONFIG_0	DO	The module is suspended	The voltage value is determined by the host end and used for M.2 port type	If not used, leave floating
69	CONFIG_1	DO	Module internal	The voltage value is determined by the host end and is used for M.2 port type	
75	CONFIG_2	DO	The module is suspended	The voltage value is determined by the host end for M.2 port type identification.	
1	CONFIG_3	DO	The module is suspended	The voltage value is determined by the host end for M.2 port type identification.	

The following is a reference circuit diagram for four configuration pins:

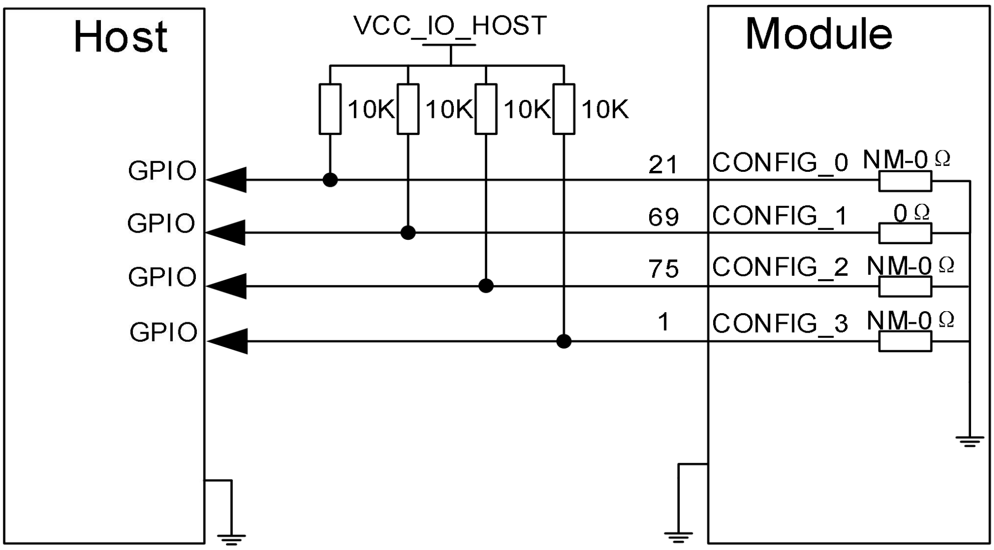


Figure 4.16 CONFIG Configuration Pin Reference Circuit

Table 4-15 Pin Configuration List of M.2 Specification

CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module types and host interfaces	Port configuration
NC	GND	NC	NC	Defined by Lierda.	N/A

4.10 ANT_CTRL interface*

The NR90-HCN M.2 module provides two ANT_CTRL interfaces for external tuners, as defined in the table below.

Table 4-16 NR90-HCN M.2 MIPI RFFE Pin Description

Pin numb	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
56	ANT_CTRL1	DO	External RF device control	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	
58	ANT_CTRL0	DO	External RF device control	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	

Note

*The interface function is under development and not yet supported, but test points can be introduced first.

4.11 Antenna interface

4.11.1 Antenna interface

NR90-HCN M.2 module provides two IPEX4 generation antenna interfaces, the positions and interface definitions are as follows:

Figure 4.17 Antenna Interface Location Diagram

Table 4-17 NR90-HCN M.2 Antenna Interface Definition

Antenna	Antenna types	Frequency band	Frequency range
M	TRx0	**WCDMA:**B1/5/8 **LTE**: B1/3/5/8/34/38/39/40/41 **NR**: n1/3/5/8/28/41/78/79	703～5000
D	Rx1	**WCDMA:**B1/5/8 **LTE**: B1/3/5/8/34/38/39/40/41 **NR**: n1/3/5/8/28/41/78/79	703～5000

When in use, the antenna can be directly led out from the antenna interface of the module, or it can be transferred via the PCB board. When transferring, the RF traces on the board should be as short as possible, and Π-type/double L matching circuits should be reserved for debugging to ensure that the trace impedance is 50Ω.

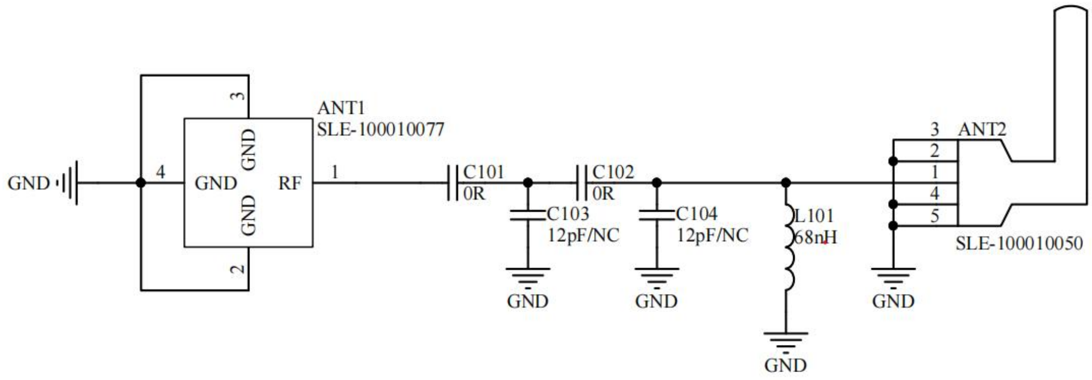


Figure 4.18 Antenna Matching Circuit

4.11.2 RF connector dimensions

The dimensions of the module antenna connector are as shown in the following figure:

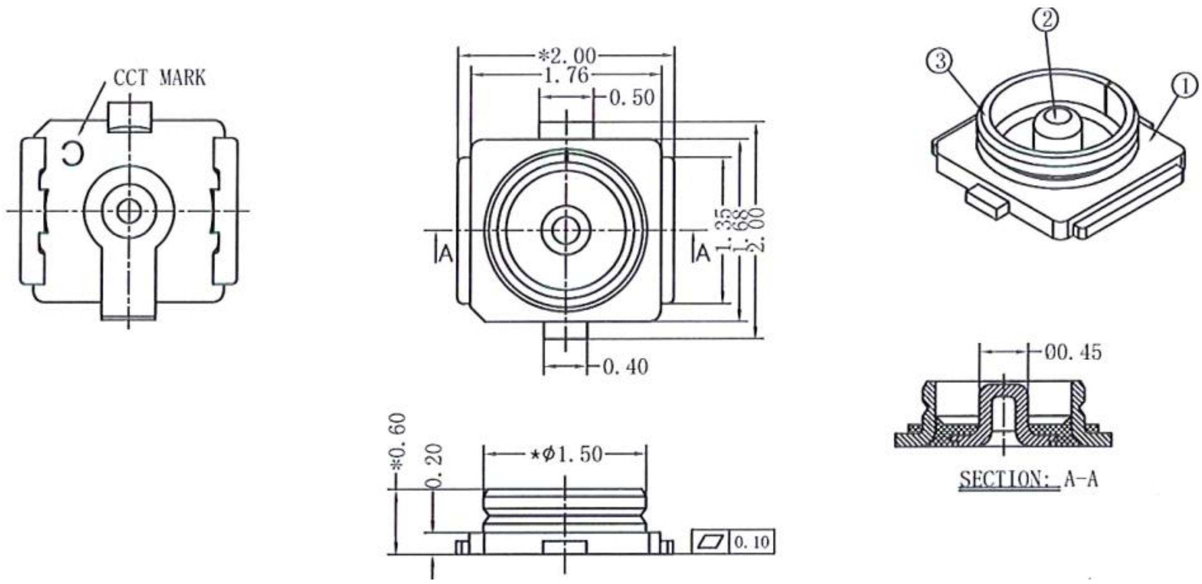


Figure 4.19 Motherboard RF Connector Dimension Diagram (unit:mm)

Table 4-18 Main Characteristics of RF Connectors

Parameters	Standard
Nominal frequency range	DC~6GHz
Characteristic Impedance	50Ω
Temperature range	-40~90℃
Voltage Standing Wave Ratio (VSWR)	Maximum 1.3 (0~3 GHz); Maximum 1.4 (3~6 GHz)

4.11.3 RF coaxial cable requirements

The selection of coaxial cables matching the RF socket is recommended to refer to the following specifications.

Table 4-19 RF Coaxial Cable Characteristics

Parameters	Standard
Nominal frequency range	DC~6GHz
Line Loss	0.1dBm/V@100MHz
Characteristic impedance	50Ω
Temperature range	-40~85℃
Voltage Standing Wave Ratio (VSWR)	Maximum 1.3 (0~3 GHz); Maximum 1.4 (3~6 GHz)

The picture shows the state after the docking of 0.81 fourth-generation and 1.13 fourth-generation.

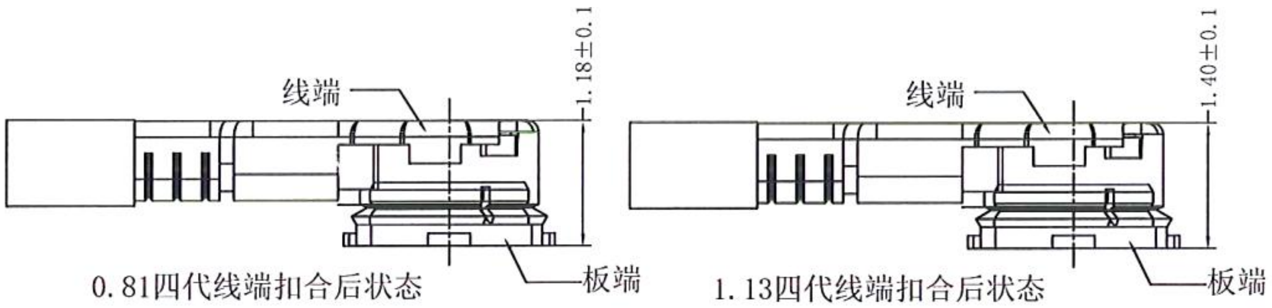


Figure 4.20 The state after the cable connector is fastened.

4.11.4 Antenna selection requirements

The passive parameter selection of the collapsible rod antenna is as follows.

Table 4-20 NR90-HCN M.2 Antenna Selection Parameters

Parameters	Standard
Frequency Range	700-5000MHz
Characteristic impedance	50Ω
Standing wave ratio	≤ 2
Efficiency	> 30%
Joint	SMA

Passive parameters are for reference only, actual selection should be based on OTA data.

5 Radio Frequency Characteristics

This chapter mainly introduces the RF characteristics of the module:

- Conduction reception sensitivity
- Transmitting power

5.1 Conducting test data

5.1.1 Test environment

Test equipment: Lierda CMW500, MT8000A

Power: 66319D

5.1.2 Conduction reception sensitivity

The receive sensitivity indicator is an important parameter for evaluating the performance of the NR90-HCN M.2 module, and the test results are shown in the table below.

Table 5-1 Description of NR90-HCN M.2 Receiver Sensitivity

Frequency band	Test value (unit: dBm)			3GPP(MIMO)
	Main Collection	Episode	MIMO	
WCDMA Band 1	-109	-110	-112.3	-106.7
WCDMA Band 5	-110	-110	-113	-104.7
WCDMA Band 8	-109	-109.5	-112	-103.8
LTE Band 1(10 MHz)	-97	-98	-100.4	-96.3
LTE Band 3(10 MHz)	-97.3	-98.3	-100.6	-93.3
LTE Band 5(10 MHz)	-99	-99	-101.4	-94.3
LTE Band 8(10 MHz)	-97.5	-99	-101.5	-93.3
LTE Band 34(10 MHz)	-97.5	-99	-101.6	-96.3
LTE Band 38(10 MHz)	-96	-97.5	-99.7	-96.3
LTE Band 39(10 MHz)	-97	-99	-101.4	-96.3
LTE Band 40(10 MHz)	-96.5	-97.5	-100.4	-96.3

Frequency band	Test value (unit: dBm)			3GPP(MIMO)
	Main Collection	Episode	MIMO	
LTE Band 41(10 MHz)	-96	-96.5	-99.1	-94.3
NR n1(20 MHz)	-93.3	-96	-97.1	-93.8
NR n3*(20 MHz)	-96.4	-95	-98.4	-90.8
NR n5*(20 MHz)	-96.2	-95	-98.5	-90.8
NR n8(20 MHz)	-94.7	-95.2	-98	-90
NR n28(20 MHz)	-96	-94.2	-98.3	-90.8
NR n41(20 MHz)	-93	-93.2	-96.3	-92
NR n78(20 MHz)	-95	-95.6	-98.2	-92.9
NR n79(20 MHz)	-94	-94.4	-97.1	-92.9

5.1.3 Transmitting power

Conduction Transmit Power is an important indicator for measuring the performance of the NR90-HCN M.2 module, and the test results are shown in the table below.

Table 5-2 NR90-HCN M.2 Transmit Power Description

Frequency band	Measurement value	3GPP
WCDMA B1	23	24dBm +1.7/-3.7dB
WCDMA B5	23	24dBm +1.7/-3.7dB
WCDMA B8	23	24dBm +1.7/-3.7dB
LTE B1	22	23dBm ±2.7dB
LTE B3	22	23dBm ±2.7dB
LTE B5	23	23dBm ±2.7dB
LTE B8	23	23dBm ±2.7dB
LTE B34	23	23dBm ±2.7dB
LTE B38	23	23dBm ±2.7dB
LTE B39	23	23dBm ±2.7dB
LTE B40	23	23dBm ±2.7dB
LTE B41 (PC3)	23	23dBm ±2.7dB
LTE B41 (PC2)	25.5	26dBm +2.7/-3.7dB(Class2)

Frequency band	Measurement value	3GPP
NR n1	22	23dBm ±2.7dB(Class 3)
NR n3*	22	23dBm ±2.7dB(Class 3)
NR n5*	23	23dBm ±2.7dB(Class 3)
NR n8	23	23dBm ±2.7dB(Class 3)
NR n28	23	23dBm +2.7/-3.2dB(Class 3)
NR n41 (PC3)	23	23dBm +2.7/-3.2dB(Class 3)
NR n78 (PC3)	23	23dBm +2.7/-3.7dB(Class3)
NR n79 (PC3)	23	23dBm +2.7/-3.7dB(Class3)

6 Electrical performance and reliability

This chapter mainly introduces the electrical characteristics and reliability characteristics of the NR90-HCN M.2 module interface.

6.1 Work and storage environment

The operating and storage temperature ranges of the NR90-HCN M.2 module are shown in the table below.

Table 6-1 NR90-HCN M.2 Operating and Storage Temperatures

Parameters	Minimum value (°C)	Maximum value (℃)
Normal operating temperature	-30	+75
Expand operating temperature.	-40	+85
Storage temperature	-40	+90

6.2 Power characteristics

The input voltage requirements for the NR90-HCN M.2 module are as shown in the table below.

Table 6-2 NR90-HCN M.2 Operating Voltage

Symbol	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Ripple (V)
VBAT	External power supply voltage	3.3	3.8	4.4	0.1

The power waveform in launch state is as shown in the following figure:

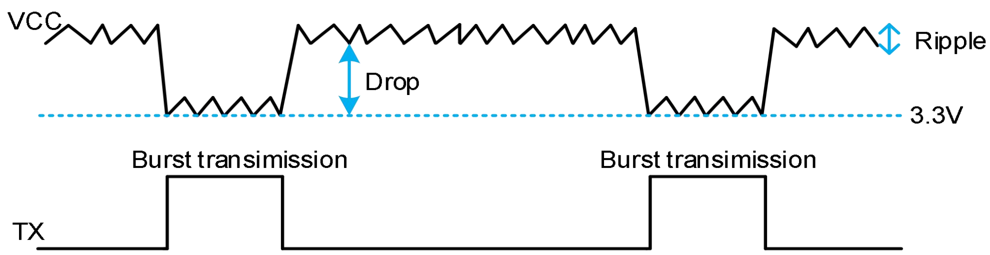


Figure 6.1 Power Requirements for RF Transmission

6.3 Absolute maximum rated value

Table 6-3 Absolute Maximum Ratings

Symbol	Minimum value	Maximum value	Unit
VBAT	-0.3	5.0	V
Digital interface voltage	-0.3	1.98	V

6.4 Power consumption characteristics

Table 6-4 Power Consumption of NR90-HCN M.2 Module

Module status	Condition	Average Typ.Current(mA)@ 3.8V
Shutdown mode	Module power off	0.0098
Sleep mode	Idle(AT+CFUN=0)	1.059
Maximum transmission power of WCDMA	WCDMA B1 CH9750@23.95dBm	622.098
	WCDMA B5 CH4182@23.58dBm	649.244
	WCDMA B8 CH2788@23.77dBm	688.587
Maximum transmitting power of LTE	LTE-FDD B1 CH18300@22.19dBm	576.313
	LTE-FDD B3 CH19575@21.85dBm	523.859
	LTE-FDD B5 CH20525@22.87dBm	513.706
	LTE-FDD B8 CH21625@23.11dBm	560.232
	LTE-TDD B34 CH36275@22.63dBm	395.069
	LTE-TDD B38 CH38000@22.72dBm	379.187
	LTE-TDD B39 CH38450@22.47dBm	362.56
	LTE-TDD B40 CH39150@22.47dBm	314.836
	LTE-TDD B41 CH39700@25.07dBm	604.399
Maximum transmission power of 5G NR	5G NR-FDD n1 CH428000@21.96dBm	528.744
	5G NR-FDD n3* CH368500@22.34dBm	584.364
	5G NR-FDD n5* CH176300@22.5dBm	502.866
	5G NR-FDD n8 CH188500@22.43dBm	515.604
	5G NR-FDD n28 CH159100@22.38dBm	568.531
	5G NR-TDD n41 CH159100@22.98dBm	251.817

	5G NR-TDD n78 CH636666@23.18dBm	269.246
	5G NR-TDD n79 CH713334@23.12dBm	244.108

6.5 ESD protection

6.5.1 ESD design recommendations

The overall ESD performance is mainly determined by: structural shielding, PCB layout protection, and device protection performance. Here are some considerations for device selection:

- Reverse leakage current IR: Excessive reverse current not only increases system power consumption but may also affect signal functionality, especially noticeable in high-speed, low-drive capability signals.
- Reverse working voltage VRWM: This voltage should be higher than the normal operating voltage at the protected network terminal;
- IPP, Clamping Voltage, and Peak Pulse Power: These three parameters follow the relationship P=UI, the smaller the clamping voltage, the safer the back-end device; ESD is easily weakened by factors such as structure, PCB capacitance, etc., so the discharged static electricity will not be fully applied to the network to be protected, making it difficult to estimate these parameters;
- Interlayer capacitance CJ: Too large interlayer capacitance will affect high-speed signal integrity;

We suggest:

(1) High-speed signal interface: CJ<1pF for USB2.0 interface

(2) Low-speed signal interface: (U)SIM interface CJ<10pF, UART interface, PCM interface CJ<20pF, TVS diodes or varistors can be used for ESD protection.

- Antenna Interface: If TVS devices are used in the antenna interface, RSE (radiated spurious emission) may exceed the value defined by EN301489. Therefore, it is not recommended to use TVS at the antenna port. It is suggested to connect an inductor of

47nH to 82nH for ESD protection.

6.5.2 ESD environmental control recommendations

(1) The processing equipment, testing instruments, tools, and equipment of electrostatic sensitive devices are all reliably grounded.

(2) The parts that come into contact with static sensitive components on devices, instruments, tools, and fixtures, as well as moving parts close to static sensitive components, are made of anti-static materials, and have good grounding. Non-antistatic material parts undergo anti-static treatment.

(3) In the process of handling electrostatic sensitive devices such as ICs, single boards, modules, etc., employees correctly wear static wrist straps or static gloves;

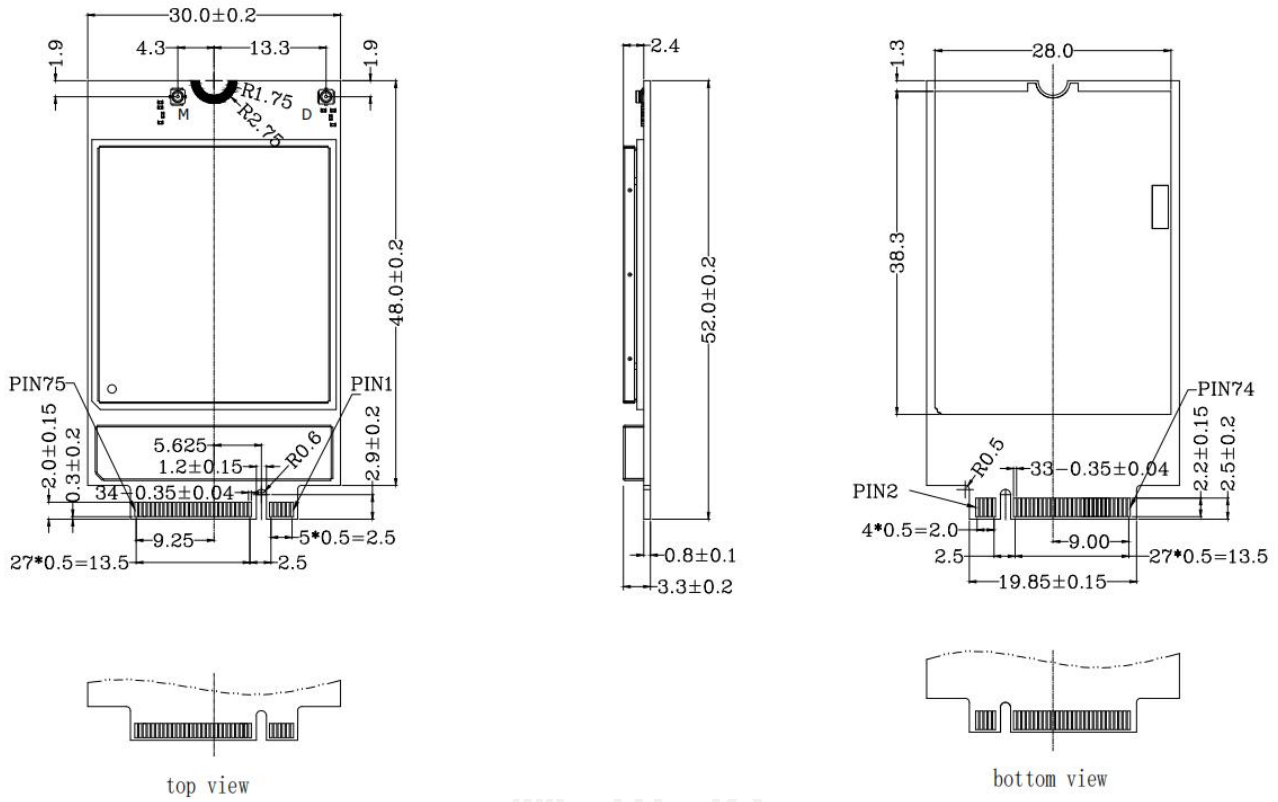
(4) Are there obvious anti-static signs and anti-static measures in the process of transporting and storing electrostatic sensitive devices?

Table 6-5 ESD Performance Parameters (Temperature: 25°C, Humidity: 40%)

Pin name	Discharge phenomenon	Air discharge
VBAT,GND	+/-4kV	+/-8kV
Antenna Interface	+/-4kV	+/-8kV
Others	+/-0.5kV	+/-2kV

7 Mechanical dimensions

7.1 Mechanical dimensions



UNIT:mm

Figure 7.1 Module Mechanical Dimensional Drawing

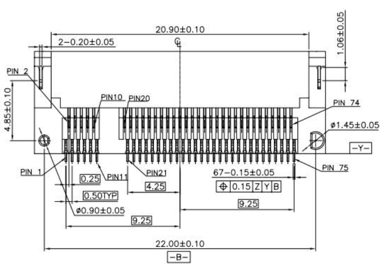
7.2 Module rendering

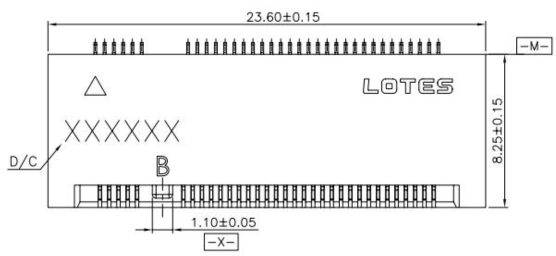
Figure 7.2 Module Rendering

The above is the design rendering of the module, please refer to the actual module for accuracy, especially the label content is for reference only.

7.3 M.2 connector

The NR90-HCN M.2 module uses a standard PCI Express M.2 connector. For more information, please refer to the PCI Express M.2 Specification Revision 3.0, Version 1.2. The following diagram shows an M.2 Key B type connector with a LOTES model number API0026-P001.





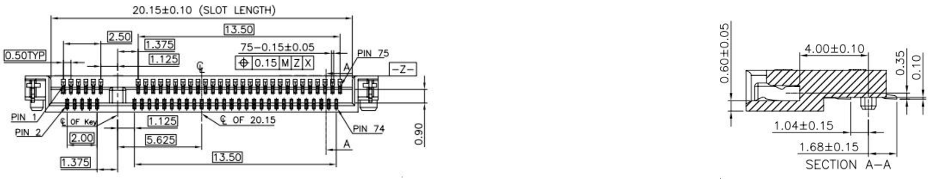


Figure 7.3 PCI Express M.2 Key B connector (Unit:mm)

8 Packaging information

The NR90-HCN M.2 module is packaged in a blister pack, the specific scheme is as follows.

8.1 Thermoformed tray

The vacuum formed tray dimensions are as follows:

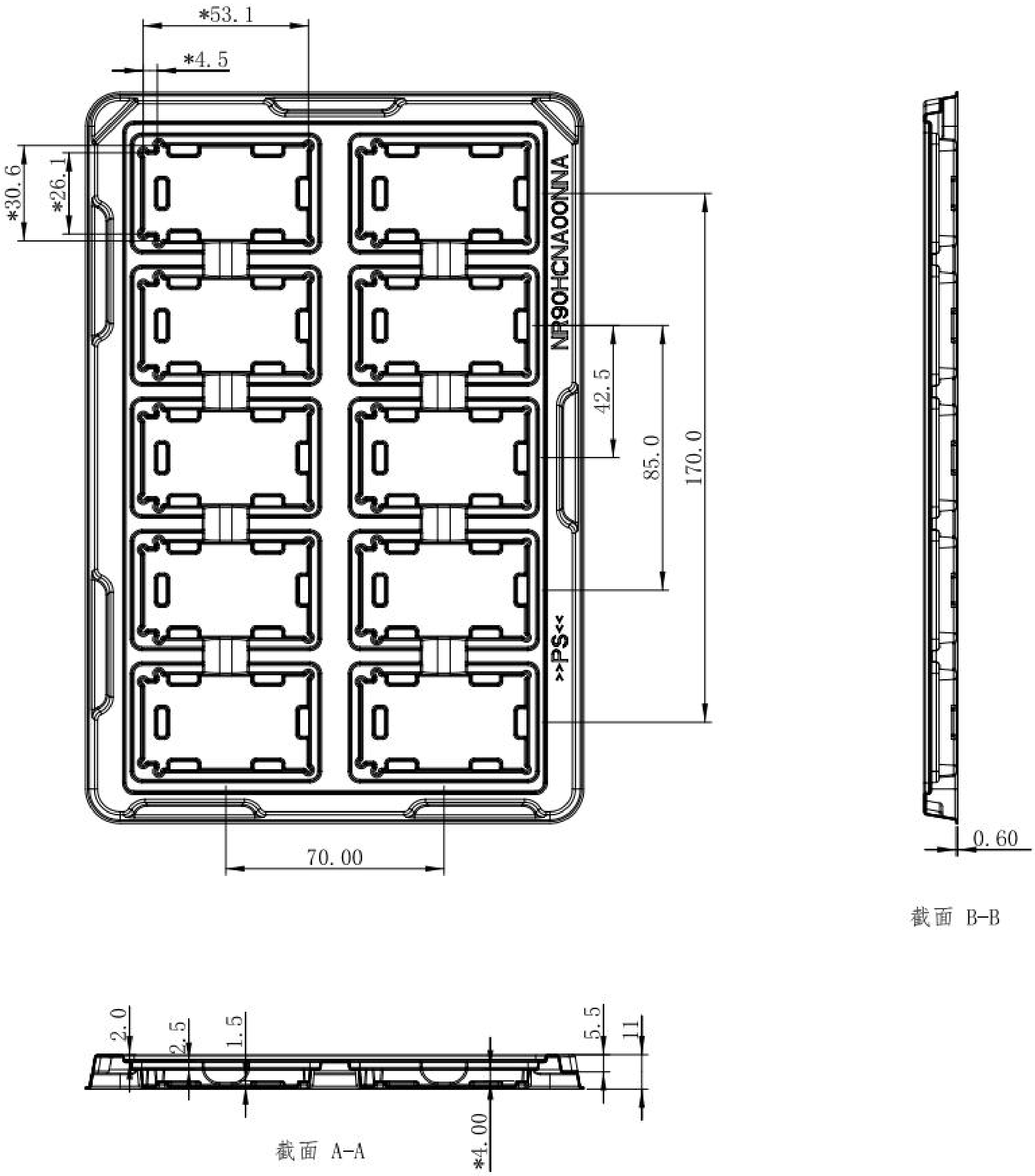
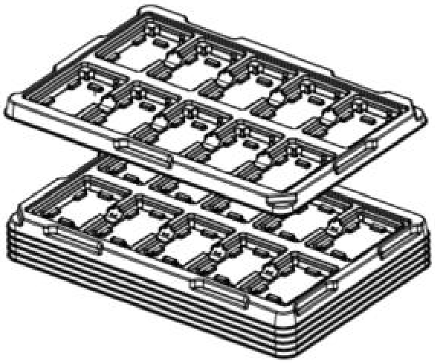


Figure 8.1 Vacuum Formed Tray Dimensional Drawing (unit:mm)

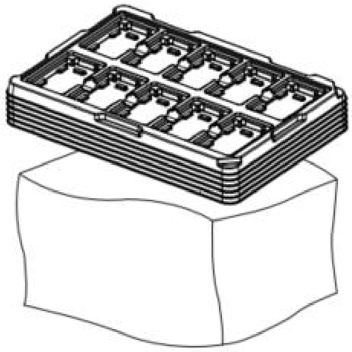
8.2 Packaging process



Each vacuum-formed tray holds 10 modules, and then 5 trays are filled.

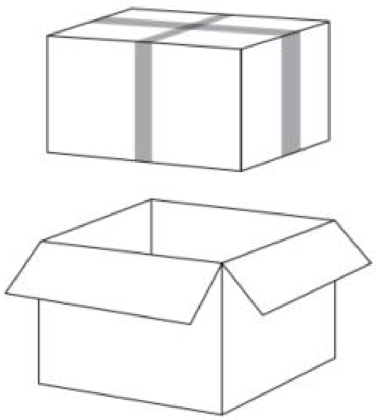
The trays of the module are stacked together, with an empty one placed on top.

Tray.



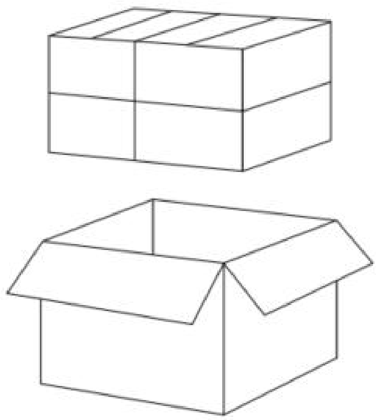
Pack 6 vacuum-formed trays together, place a piece of cardboard on the top and bottom, add 10 grams of desiccant, then put the vacuum-formed trays into an aluminum foil bag, vacuum seal, and pack.

Lierda



Put the sealed vacuum-formed tray into a small box, one small box can contain

Install 50 modules.



Put 4 small boxes into one cardboard box and seal it. One cardboard box can pack 200 modules.

Figure 8.2 Packaging Process

9 Relevant documents and terminology abbreviations

Table 9-1 Related Documents

Serial number	Document Name	Annotation
[1]	Lierda NR90-HCN AT Command Manual_Rev 1.2	AT command set

Table 9-2 Term Abbreviations

Abbreviation	Full English name	Full name in Chinese
bps	bits per second	Per second
CPE	Customer-Premise Equipment	User resident equipment
FOTA	Firmware Over-The-Air	Firmware over-the-air differential upgrade
ESD	Electrostatic Discharge	Electrostatic discharge
FDD	Frequency Division Duplexing	Frequency Division Multiplexing
HSPA	High Speed Packet Access	High-speed data packet access
HSUPA	High Speed Uplink Packet Access	High-speed uplink data packet access
kbps	Kilo Bits Per Second	Thousand bits per second
LED	Light Emitting Diode	Light Emitting Diode
LTE	Long Term Evolution	Long-term evolution
Mbps	Mega Bits Per Second	Megabits per second
MIMO	Multiple-Input Multiple-Output	Many inputs, many outputs

Lierda 利 尔 达

Abbreviation	Full English name	Full name in Chinese
NR	New Radio	New Air Interface
PCIe	Peripheral Component Interconnect Express	Peripheral component interconnect standard
PCM	Pulse Code Modulation	Pulse Code Modulation
PPP	Point-to-Point Protocol	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation	Orthogonal Amplitude Modulation
QPSK	Quadrature Phase Shift Keying	Quadrature Phase Shift Keying
RC	Root Complex	Root complex
RF	Radio Frequency	Radio Frequency
RFFE	RF Front-End	RF front end
Rx	Receive	Receive
SIMO	Single Input Multiple Output	Single Input Multiple Output
SMS	Short Message Service	Short Message Service
Tx	Transmit	Send
UART	Universal Asynchronous Receiver & Transmitter	Universal asynchronous transmitter/receiver
USB	Universal Serial Bus	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module	(Global) User Identification Module
VIH	Input High Voltage Level	Enter high voltage level
VIL	Input Low Voltage Level	Input low voltage level
VOH	Output High Voltage Level	Output high voltage level
VOL	Output Low Voltage Level	Output low voltage level
WCDMA	Wideband Code Division Multiple Access	Broadband code division

Abbreviation	Full English name	Full name in Chinese
		multiple access