Lierda NR90-HEA Module Hardware Design Manual

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Revision History of the Document

Document Version	Change Date	Reviser	Reviewer	Change content
Rev1.0	24-10-27	CHB		Initial Version
Rev1.1	24-12-20	CHB		1、Modify frequency band support information 2、Update the laser screen printing schematic.
Rev1.2	25-04-10	CHB		Increase n40
Rev1.3	25-04-25	CHB		Standardization optimization of documents

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	Please turn off your mobile devices before boarding. The wireless function of mobile devices is prohibited from being turned on during the flight to prevent interference with the aircraft communication system. Ignoring this prompt may compromise flight safety and even violate the law.
	When in a hospital or healthcare facility, pay attention to any restrictions on the use of mobile terminal devices. RF interference can cause medical equipment to malfunction, so it may be necessary to turn off mobile terminal devices.
	Mobile terminal devices do not guarantee effective connection in all situations, such as when there is no credit on the mobile terminal device or the SIM card is invalid. In case of emergency situations with the above conditions, remember to use emergency calls, and ensure that your device is powered on and in an area with sufficient signal strength.
	Your mobile terminal device will receive and emit radio frequency signals when powered on, which may cause radio frequency interference when close to a TV, radio, computer, or other electronic devices.
	Please keep mobile terminal devices away from flammable gases. When you are near gas stations, oil depots, chemical plants, or explosive operation sites, please turn off mobile terminal devices. Operating electronic devices in any potentially explosive environment poses a safety hazard.

Module selection for application

Serial number	Module model	Feature symbol	Support frequency band	Dimensions	Module introduction
1	NR90-HEA	NNC	WCDMA/LTE/NR	32*29*2.4mm	5G RedCap module

Content

1 Introduction

This document defines the hardware application specification of the Lierda Group's NR90-HEA 5G RedCap module, describing its hardware interfaces, electrical characteristics, application methods, mechanical specifications, and other content.

This document can help users quickly understand the hardware interface specifications, electrical, mechanical characteristics, and other relevant information of the module. Combined with other corresponding documents, users can quickly master the application methods of the 5G module.

2 Product Overview

Lierda NR90-HEA 5G RedCap series module is designed for high-reliability, low-latency, large-connection, medium-to-high-speed application scenarios. It is based on 3GPP Release 17 technology, supports 5G Standalone (SA) mode, is compatible with LTE network standards, and meets the frequency band requirements of the four major domestic operators. It supports 5G LAN, high-precision 5G network timing, multi-network slicing, high-precision NR positioning, uRLLC, SUL, and other 5G features.

The NR90-HEA module uses the LGA+LCC interface, with dimensions of 32*29*2.4mm. The module supports 1T2R and is also compatible with 1T1R. The module provides a variety of functional interfaces, supporting USB, RGMII, UART, SPI, SDIO, etc., making it convenient for users to expand peripherals. It can adapt to various types of operating systems (Android, Linux, Windows, etc.) and supports multiple drivers and network protocols.

The NR90-HEA module is a surface-mounted module with a total of 144 LGA+LCC package pins.

The NR90-HEA module is an industrial-grade module, only suitable for industrial and commercial applications.

The NR90-HEA module can be applied in the following terminal scenarios:

- Intelligent Industry
- Energy and Power
- Video surveillance
- Mobile broadband
- Connected Vehicles
- Smart wearables

2.1 Frequency bands and functions

The frequency bands supported by the NR90-HEA module are as shown in the table below:

Table 2-1 Description of Frequency Bands Supported by NR90-HEA Module

Frequency band	Launch	Receive
WCDMA Band 1	1920MHz-1980MHz	2110MHz-2170MHz
WCDMA Band 5	824MHz-849MHz	869MHz-894MHz
WCDMA Band 8	880MHz-915MHz	925MHz-960MHz
FDD LTE Band 1	1920MHz-1980MHz	2110MHz-2170MHz
FDD LTE Band 3	1710MHz-1785MHz	1805MHz-1880MHz
FDD LTE Band 5	824MHz-849MHz	869MHz-894MHz
FDD LTE Band 7	2500MHz-2570MHz	2620MHz-2690MHz
FDD LTE Band 8	880MHz-915MHz	925MHz-960MHz
TDD LTE Band 20	832MHz-862MHz	791MHz-821MHz
TDD LTE Band 28	703MHz-748MHz	758MHz-803MHz
TDD LTE Band 38	2570MHz-2620MHz	2570MHz-2620MHz
TDD LTE Band 40	2300MHz-2400MHz	2300MHz-2400MHz
TDD LTE Band 41	2496MHz-2690MHz	2496MHz-2690MHz
TDD LTE Band 42	3400MHz-3600MHz	3400MHz-3600MHz
TDD LTE Band 43	3600MHz-3800MHz	3600MHz-3800MHz
NR n1	1920MHz-1980MHz	2110MHz-2170MHz
NR n3	1710MHz-1785MHz	1805MHz-1880MHz
NR n5	824MHz-849MHz	869MHz-894MHz
NR n7	2500MHz-2570MHz	2620MHz-2690MHz
NR n8	880MHz-915MHz	925MHz-960MHz
NR n20	832MHz-862MHz	791MHz-821MHz
NR n28	703MHz-748MHz	758MHz-803MHz
NR n40	2300MHz-2400MHz	2300MHz-2400MHz
NR n41	2496MHz-2690MHz	2496MHz-2690MHz
NR n77	3300MHz-4200MHz	3300MHz-4200MHz
NR n78	3300MHz-3800MHz	3300MHz-3800MHz

2.2 Key Features

The NR90-HEA module adopts 3GPP Rel-17 technology, supports 5G Standalone (SA) networking, and can meet the requirements of vertical industries such as smart industry and energy power. The table below shows the main features of the NR90-HEA module.

Table 2-2 Main Characteristics of the NR90-HEA Module

Type	Description
Encapsulation	LGA+LCC
Physical properties	Dimensions: 32*29*2.4mm Weight: approximately 5.10g
CPU frequency	750MHz
Transmission rate (theoretical value)	SA DL：226Mbps；UL：120Mbps LTE DL：200Mbps；UL：100Mbps WCDMA DL：384kbps；UL：384kbps
Transmit power	WCDMA：Class 3 (24dBm +1.7/-3.7dB) LTE B1/B3/B5/B7/B8/B20/B28/B38/B40/B42/B43： Class 3 (23dBm ±2.7dB) LTE B41：Class 2 (26dBm +2.7/-3.7dB) 5G NR n1/n3/n5/n7/n8/n20/n28/n40/n41/n77/n78：Class 3(23dBm ±2.7dB)
WCDMA Features	Support 3GPP FDD R6 version protocol Maximum transmission rate (theoretical value): WCDMA: 384kbps (downlink speed) / up to 384kbps (uplink speed)
LTE features	Support 3GPP Release 13 protocol. Support LTE FDD/TDD Support CAT4 Support 1.4/3/5/10/15/20 MHz RF bandwidth. Support uplink QPSK, 16QAM, 64QAM, 256QAM modulation modes. Support QPSK, 16QAM, 64QAM, and 256QAM modulation schemes. Support downlink 2×2 MIMO. Maximum transmission rate (theoretical value): LTE: 200Mbps (downlink speed) / 100 Mbps (uplink speed)
5G NR features	Support 3GPP R17 protocol version. Support uplink 256QAM modulation and downlink 256QAM modulation. n1/n3/n5/n7/n8/n20/n28/n40/n41//n77/n78 support downlink 2×2 MIMO Support 15kHz and 30kHz for SCS. Support SA working mode Support Option 3x, 3a, 3 and Option 2 Maximum transmission rate (theoretical value, related to network

Type	Description
	configuration and heat dissipation environment): SA: 226Mbps (average downlink speed) / 120Mbps (average uplink speed)
Operating voltage range	DC 3.3V ~ 4.4V (typical value 3.8V)
Application temperature range	Operating temperature: -10 ~ +55℃ Operating Temperature: -40 ~ +85°C Storage Temperature: -40 ~ +90°C
AT command	Refer to the detailed design document for the NR90-HEA AT command.
USB interface	USB2.0 (High Speed) interface, with a maximum speed of up to 480Mbps.
UART interface	Main serial port: used for data transmission and AT commands Debug serial port: partial log output
(U)SIM interface	1 standard SIM interface (Class B and Class C)
PCM and I2S interfaces	1-way PCM (I2S) interface, supports voice Support expanding Codec or SLIC.
SPI interface	Implement SLIC function with PCM interface
I2C interface	Support standard and fast modes
PCIe interface	Compliant with PCIe 1.1 specification, with a transfer rate of up to 2.5Gbps.
B code output interface	B_CODE×1；1 PPS_OUT×1；
Control Indication Interface	WAKEUP_SLEEP_IN AP_READY W_DISABLE# STATUS RESET_N USB_BOOT PWRKEY WAKE_OUT
Antenna interface	ANT*2
Network Protocol	PPP/RNDIS/ECM TCP/IP MQTT
Drive	linux2.6-5.10 Andriod4. x-10. x Windows7/8/8.1/10
AT	Support AT commands compliant with 3GPP standards.
FOTA	Support
OneNET	Support
Certification	CCC/SRRC/NAL/RoHS/CE*/Operator Certification* (Telecom/Unicom/Mobile)

Note

In development

2.3 Function Block Diagram

The diagram illustrates the main functions of the NR90-HEA module: power management, baseband section, memory, RF functions, peripheral interfaces.

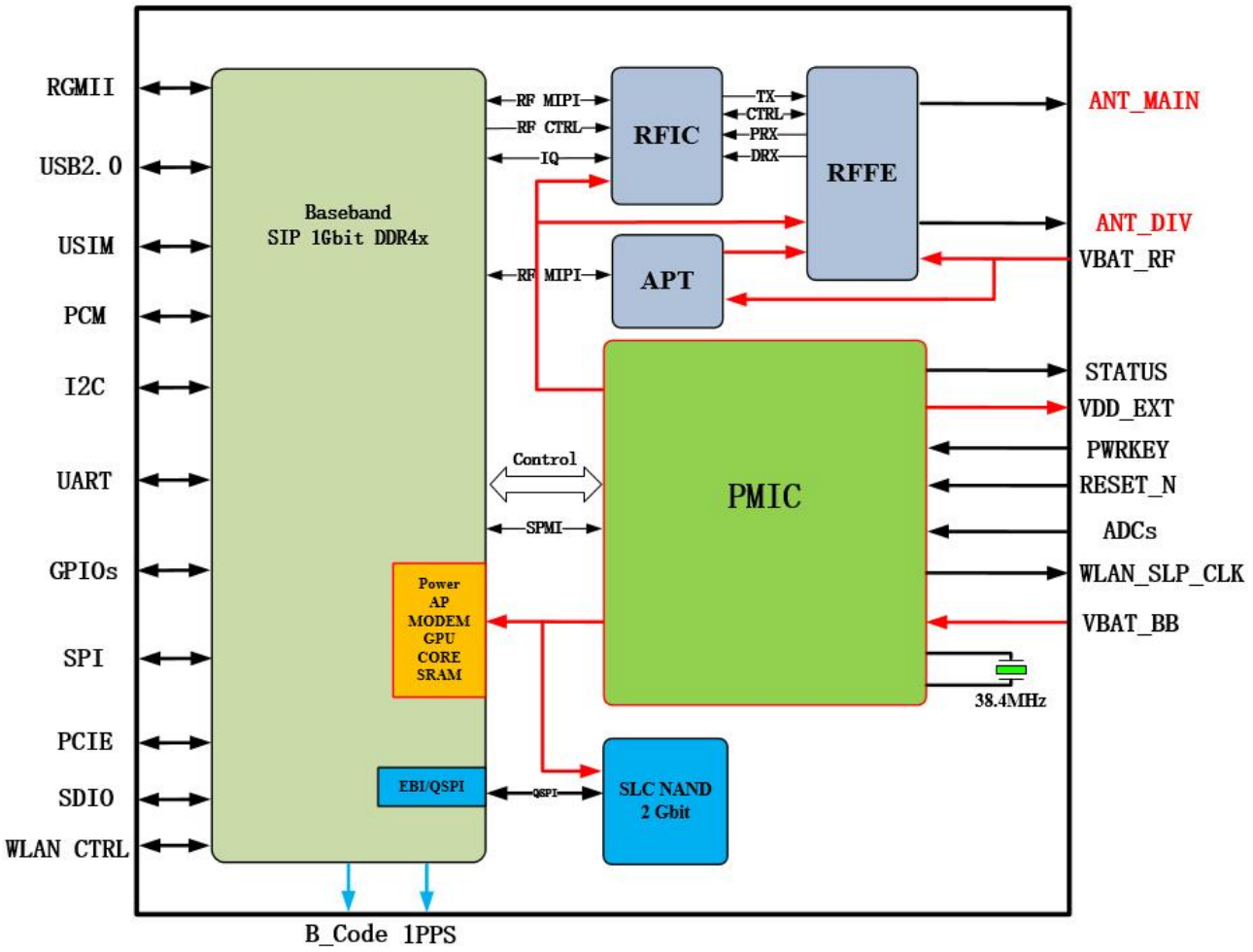


Figure 2.1 Hardware Block Diagram of NR90-HEA Module

2.4 Pinout diagram

The following is the pin assignment diagram for the NR90-HEA module interface.

Figure 2.2 Module Pinout Diagram

2.5 Pin Description Table

Table 2-3 I/O Type Definitions

Type	Description
PI	Power input signal
PO	Power output signal
DI	Digital input signal
DO	Digital output signal
AI	Simulated input signal
AO	Simulated output signal
DIO	Dual-directional digital input/output signal
OD	Leakage opens the way
VIL	Low-level input voltage
VIH	High-level input voltage
VOL	Low-level output voltage
VOH	High-level output voltage

Table 2-4 Pin Definitions

Pin Names	Pin number	Note
GND	8, 9, 10,19, 22, 36, 46, 48, 50~54, 56, 72, 85~112	Keep grounded.
NC	34, 43, 47, 55, 123, 128 ~134, 142	Keep hanging

Table 2-5 Pin Definitions

Pin	Pin Names	Type	Description	Note
1	WAKEUP_SLEEP_IN	DI	Module sleep mode control, low effective	1.8V always-on domain
2	AP_READY	DI	AP sleep state detection	1.8V
3	B_CODE	DO	B code output, high-precision time synchronization	1.8V constant-on domain
4	W_DISABLE#	DI	Module flight mode control, low effective	1.8V constant-on domain

Pin	Pin Names	Type	Description	Note
5	NET_MODE	DO	Network registration status of the instruction module	1.8V
6	NET_STATUS	DO	Network operation status of the instruction module	1.8V
7	VDD_EXT	PO	Output 1.8V power supply externally	1.8V output, 50mA Max
11	DBG_RXD	DI	AO_UART_RXD	1.8V constant-on domain
12	DBG_TXD	DO	AO_UART_TXD	1.8V always-on domain
13	USIM_DET	DI	(U)SIM card detection	1.8V constant-on domain
14	USIM_VDD	PO	(U)SIM card power	1.8V/3V Adaptive
15	USIM_DATA	DIO	(U)SIM card data	
16	USIM_CLK	DO	(U)SIM card clock	
17	USIM_RST	DO	(U)SIM card reset	
18	SIM_SWITCH	DO	SIM card switch enable, default low	1.8V
20	RESET_N	DI	Module reset signal, active low	1.8V
21	PWRKEY	DI	Module power on/off signal, low active	1.8V
23	GPIO_01	IO	General GPIO, sleep not available	1.8V
24	PCM_IN	DI	PCM data input	1.8V
25	PCM_OUT	DO	PCM data output	1.8V
26	PCM_SYNC	DO	PCM synchronous signal output	1.8V
27	PCM_CLK	DO	PCM clock signal	1.8V
28	SDC_DATA3	DIO	SDIO bus DATA3	1.8V
29	SDC_DATA2	DIO	SDIO bus DATA2	1.8V
30	SDC_DATA1	DIO	SDIO bus DATA1	1.8V

Pin	Pin Names	Type	Description	Note
31	SDC_DATA0	DIO	SDIO bus DATA0	1.8V
32	SDC_CLK	DO	SDIO bus clock	1.8V
33	SDC_CMD	DIO	SDIO bus command	1.8V
35	ANT_DIV	AIO	Episode antenna	
37	SPI_CS_N	DO	SPI slave selection	1.8V
38	SPI_MOSI	DO	SPI master output/slave input	1.8V
39	SPI_MISO	DI	SPI Master In/Slave Out	1.8V
40	SPI_CLK	DO	SPI serial clock	1.8V
41	I2C_SCL	OD	I2C clock	1.8V
42	I2C_SDA	OD	I2C data	1.8V
44	ADC1	AI	Universal Serial Bus Interface 1	0-1.75V
45	ADC0	AI	Universal Serial Interface 0	0-1.75V
49	ANT_MAIN	AIO	Main antenna	
57	VBAT_RF	PI	Radio frequency power input	3.3V-4.4V, typical value 3.8V
58	VBAT_RF	PI	RF power input	3.3V-4.4V, typical value 3.8V
59	VBAT_BB	PI	Baseband power input	3.3V-4.4V, typical value 3.8V
60	VBAT_BB	PI	Baseband power input	3.3V-4.4V, typical value 3.8V
61	STATUS	OD	Indicate the module's operating status.	SINK, module working status indicator.
62	MAIN_RI*	DO	The module outputs a ringing	1.8V
63	MAIN_DCD*	DO	Module main serial port output carrier detection	1.8V
64	MAIN_CTS	DO	Module clear to send	1.8V
65	MAIN_RTS	DI	DTE requests to send data	1.8V

Pin	Pin Names	Type	Description	Note
66	MAIN_DTR*	DI	DTE ready, sleep mode control	1.8V Always-On Domain
67	MAIN_TXD	DO	Module main serial port sends data	1.8V
68	MAIN_RXD	DI	Module main serial port receives data	1.8V
69	USB_DP	AIO	USB differential data positive signal	
70	USB_DM	AIO	USB differential data negative signal	
71	USB_VBUS	PI	USB power, used for USB detection	5V, detection function only
73	RGMII_RX_D1	DI	RGMII Rcevice DATA1	1.8V
74	RGMII_RX_EN	DI	RGMII Rcevice EN	1.8V
75	RGMII_RX_CLK	DI	RGMII Rcevice CLK	1.8V
76	RGMII_RX_D0	DI	RGMII Rcevice DATA0	1.8V
77	RGMII_TX_D0	DO	RGMII Transmit DATA0	1.8V
78	RGMII_TX_D1	DO	RGMII Transmit DATA1	1.8V
79	RGMII_RX_D2	DI	RGMII Rcevice DATA2	1.8V
80	RGMII_TX_D2	DO	RGMII Transmit DATA2	1.8V
81	RGMII_TX_EN	DO	RGMII Transmit EN	1.8V
82	RGMII_RX_D3	DI	RGMII Rcevice DATA3	1.8V
83	RGMII_TX_CLK	DO	RGMII Transmit CLK	1.8V
84	RGMII_TX_D3	DO	RGMII Transmit DATA3	1.8V
113	GPS_RXD	DI	GPS serial port RX signal	1.8V
114	GPS_TXD	DO	GPS serial port TX signal	1.8V
115	USB_BOOT	DI	Forced download, low efficiency	1.8V
116	1PPS_OUT	DO	1PPS output, timing function	1.8V constant-on
117	BT_EN	DO	BT enable	1.8V

Pin	Pin Names	Type	Description	Note
118	WLAN_SLP_CLK	AO	External 32.768K clock output	Default closed
119	RGMII_RST_N	DO	PHY device reset signal, active low	1.8V
120	EPHY_INT_N	DI	Interrupt signal in PHY devices	1.8V
121	RGMII_MDIO	OD	MDIO interface data input/output signal	1.8V
122	RGMII_MDC	DO	MDIO interface clock output	1.8V
124	PCIE_PERST_N	DIO	PCIE global reset signal, active low.	1.8V
125	WLAN_EN	DO	Enable WLAN module	1.8V
126	PCIE_RX_M	AI	PCIE differential input M	1.8V
127	PCIE_RX_P	AI	PCIE differential input P	1.8V
135	WAKE_ON_WIRELESS	DI	WLAN wake-up module	1.8V constant-on domain
136	PCIE_REFCLK_M	AIO	PCIE reference clock M	1.8V
137	PCIE_REFCLK_P	AIO	PCIE reference clock P	1.8V
138	PCIE_TX_M	AO	PCIE differential output M	1.8V
139	PCIE_TX_P	AO	PCIE differential output P	1.8V
140	PCIE_CLKREQ_N	OD	PCIe clock request	1.8V
141	WAKE_OUT	DO	Module wakes up the host, low effective	1.8V
143	RFIO_1	DIO	RF antenna tuning switch control 1	Default closed
144	RFIO_2	DIO	RF antenna tuning switch controls 2	Default closed

2.6 Evaluation Suite

Lierda can provide a complete evaluation and development kit, including an ADP board for easy debugging of the minimum system, an EVB board containing peripherals such as audio, RS485, SLIC, WIFI, etc., for development convenience.

3 Working characteristics

3.1 Description of working mode

Table 3-1 Module Operation Modes Description

Working mode	Function	
Normal working mode	IDLE	The software is running normally. The module is registered on the network and can receive and send data.
	Talk/Data	The network connection is working normally. In this mode, the module's power consumption depends on the network settings and data transfer rate.
Minimum Function Mode	When the power supply is uninterrupted, using AT+CFUN=0 can set the module to the minimum functionality mode. In this mode, the RF does not work.	
Airplane mode	AT+CFUN=4 or pulling down the W_DISABLE# pin can set the module to flight mode. In this mode, the RF does not work.	
Sleep mode	In this mode, the power consumption of the module will be reduced to a very low level, but the module can still receive paging, SMS, calls, and TCP/UDP data.	
Shutdown mode	In this mode, the PMU stops supplying power to the baseband and RF sections, the software stops working, and the serial port is not accessible.	

3.2 Hibernate/Sleep Mode

In sleep mode, the DRX function of the module can reduce the power consumption of the module and broadcast the DRX index cycle value through the wireless network. The following figure shows the relationship between DRX operation time and the current consumption in module sleep mode. The longer the DRX sleep cycle, the lower the power consumption.

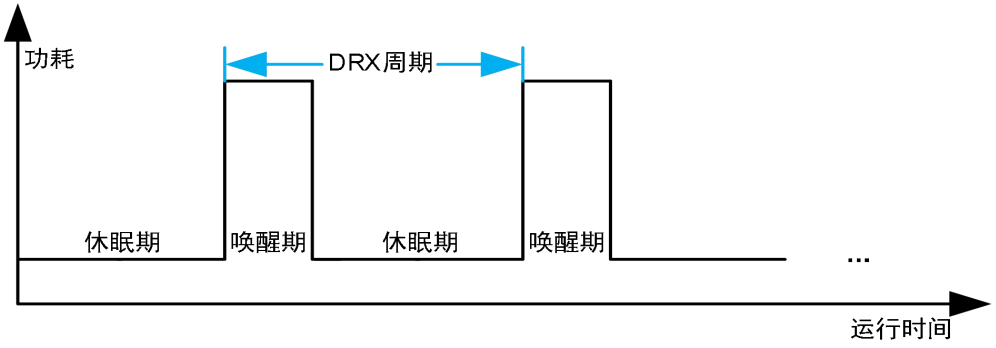


Figure 3.1 The Relationship between DRX Operating Time and Power Consumption in Sleep Mode

The process of entering and exiting sleep mode for the NR90-HEA module is as follows:

- When the module is in the wake-up state, the host pulls down the WAKEUP_SLEEP_IN pin through a GPIO, and this GPIO can remain at a low level during sleep mode.
- The module is in sleep mode, the host pulls up the WAKEUP_SLEEP_IN pin through a GPIO, and this GPIO can remain at a high level in the wake-up state.

The reference design of the WAKEUP_SLEEP_IN interface is as follows.

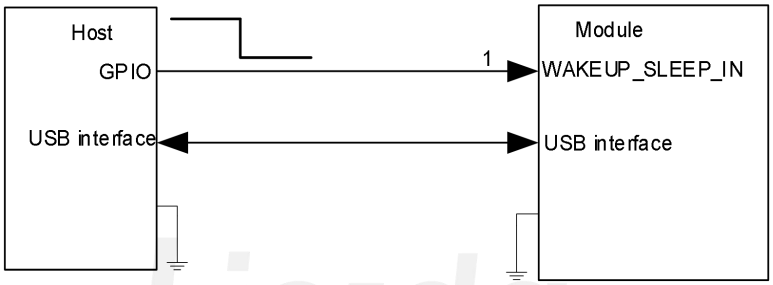


Figure 3.2 WAKEUP_SLEEP_IN Interface Reference Design Circuit

The host can pull up WAKEUP_SLEEP_IN through a GPIO to wake the module up from sleep mode.

3.2.1 Serial port application scenarios

When the module is connected to the host computer via the serial port, you can enter sleep mode by following these steps:

- Enable sleep function by using the AT+LSCLK=1 command.
- Lower WAKEUP_SLEEP_IN

The awakening steps are as follows:

- The host computer pulls up WAKEUP_SLEEP_IN and keeps it high.

3.2.2 USB application scenarios

When the module is connected to the host computer via USB, you can enter sleep

mode by following these steps:

- Enable sleep mode via the AT+LSCLK=1 command.
- Lower WAKEUP_SLEEP_IN
- Disconnect USB_VBUS power supply

The awakening steps are as follows:

- Inserting USB_VBUS can wake up the module.

3.3 Flight mode

The NR90-HEA module can control the flight mode by using the W_DISABLE# pin, and the flight mode can also be turned on or off by AT commands. When the module enters flight mode, the RF function cannot be used, and all AT commands related to RF are not accessible. The details are as follows:

Table 3-2 Module supports two ways to enter flight mode.

Serial number	Control mode	Control operation
1	Hardware I/O interface Key control	Pull up or hover (default high) W_DISABLE# for normal mode, pull down for flight mode
2	AT command control	AT+CFUN=4--Enter flight mode AT+CFUN=0--Minimum functionality mode (RF and SIM card turned off) AT+CFUN=1--Full functionality mode

Hardware method:

W_DISABLE# pin default state is high level, pulling down this pin can put the module into flight mode.

Table 3-3 W_DISABLE# Pin Description

Pin number	Pin names	Typ e	Description	Parameters	Note
4	W_DISABL	DI	Module flight mode	1.8V voltage	If not used, leave

The reference design of the W_DISABLE# interface is as shown in the following figure.

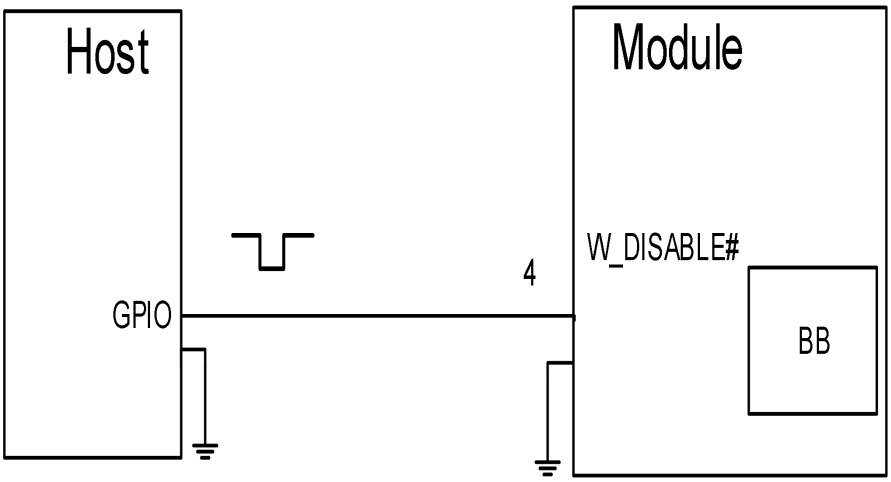


Figure 3.3 W_DISABLE# Interface Reference Circuit

3.4 Power supply design

3.4.1 Power interface

The module has 4 VBAT pins for connecting external power, which can be divided into two voltage domains:

2 VBAT_RF pins are used to supply RF power to the module.

2 VBAT_BB pins are used to supply power to the baseband of the module.

An external power supply is reserved for one channel in addition in the module. VDD_EXT is turned on by default for direct use.

Table 3-4 Power Supply Pin Definitions

Pin number	Type	Pin names	Description	Minimum value	Typical value	Maximum value	Unit
59,60	PI	VBAT_BB	Baseband section power supply	3.3	3.8	4.4	V
57,58	PI	VBAT_RF	RF power supply	3.3	3.8	4.4	V
7	PO	VDD_EXT	External 1.8V power supply 50mA Max	-	1.80	-	V

3.4.2 Power supply design requirements

To ensure the normal operation of the NR90-HEA module, the system power supply

VBAT needs to be maintained within the range of 3.3V-4.4V (typical value 3.8V). When the module is used with different external devices, attention should be paid to the power supply design of the module. In any case, it is necessary to ensure that the module's power supply voltage remains above 3.3V, otherwise the module will not function properly, and it is also recommended that the Ripple be less than 0.1V.

The power supply requires a waveform as shown in the following figure:

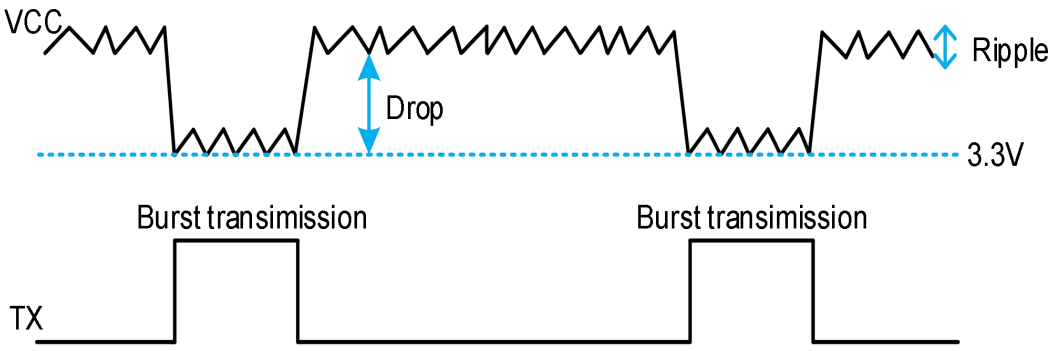


Figure 3.4 Power Requirements During Operation

External power LDO or DCDC selection advice for components capable of providing a current of 3A or more, in addition, to minimize the impact of PCB traces on power supply, VBAT_BB and VBAT_RF should adopt star routing, the width of VBAT_BB trace should not be less than 2mm, and the width of VBAT_RF trace should not be less than 2.5mm. In principle, the longer the VBAT trace, the wider the trace width.

3.4.3 Recommend design and reference circuit.

To reduce voltage drops, it is necessary to parallel at least one 220uF energy storage capacitor on VBAT_BB and VBAT_RF respectively, and reserve 3 ceramic capacitors for VBAT_BB and VBAT_RF respectively, with the capacitors placed close to the power supply pins. Additionally, to improve the stability of the power supply, it is recommended to add TVS diodes near VBAT.

Table 3-5 Capacitor Description

Recommend capacitors	Application	Explanation
220uF×2	Stabilizing tantalum capacitor	Reduce power supply fluctuations during module operation, requiring the use of low ESR (ESR=0.7Ω) capacitors. (1) The power supply requirements for LDO or DCDC should not be less than 440uF capacitance. (2) The battery power supply can be appropriately reduced to 100-220uF capacitance.
1uF，100nF	Digital Signal Noise	Filter out interference generated by clocks and digital signals.
33pF	700, 850/900MHz frequency band	Filter out low-frequency RF interference.
8.2pF	1700/1800/1900, 2100/2300, 2500/2600MHz frequency bands	Filter out RF interference in the mid/high-frequency bands.

The reference circuit is as shown in the figure below.

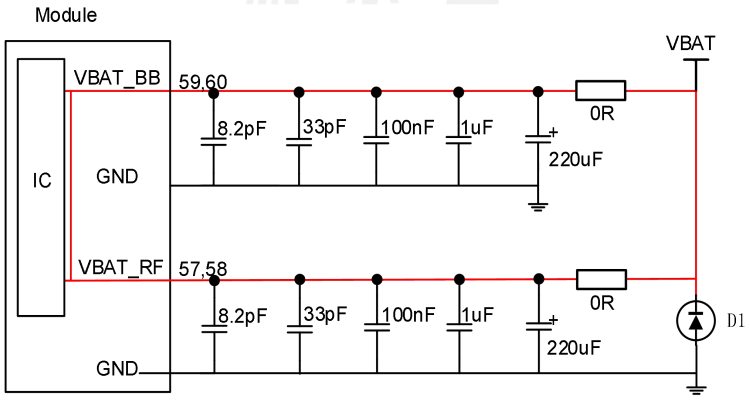


Figure 3.5 Power Supply Recommended Design

3.5 Power on/off

The NR90-HEA module implements power on and off through the PWRKEY pin.

Table 3-6 PWRKEY Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
21	PWRKEY	DI	Module power on/off control	VIH	1.5	-	1.8	Low level / low level pulse valid. Pull up to 1.8V inside the module by 10K.
				VIL	-	-	0.2	

3.5.1 Power on.

When the NR90-HEA module is in power-off mode, the module can be powered on by pulling down the PWRKEY for at least 100ms, which can be done using a GPIO signal or a button.

After pulling down PWRKEY for 100ms, the module will power on, then pull up PWRKEY.

- The host powers on by pulling down the PWRKEY pin through GPIO, the reference circuit is shown below.

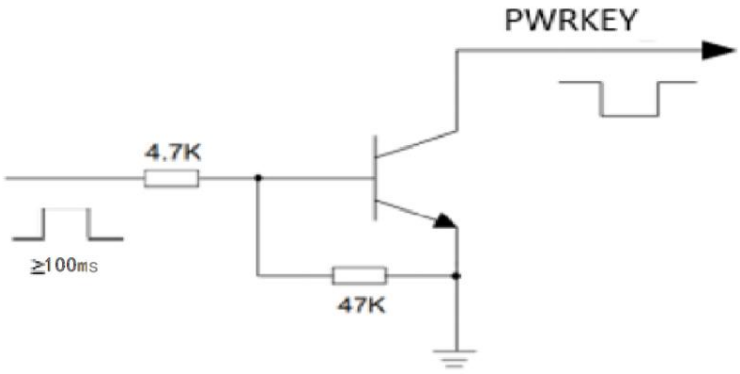


Figure 3.6 GPIO control module boot-up

- Power on is achieved by connecting the PWRKEY pin, with TVS reserved for ESD protection, refer to the circuit below.

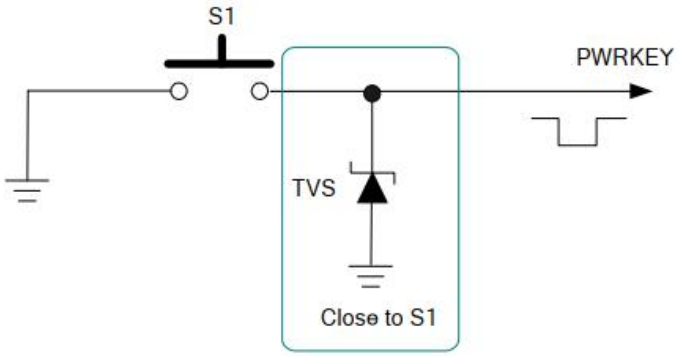


Figure 3.7 Power On Button

The power-on sequence is as shown in the following figure.

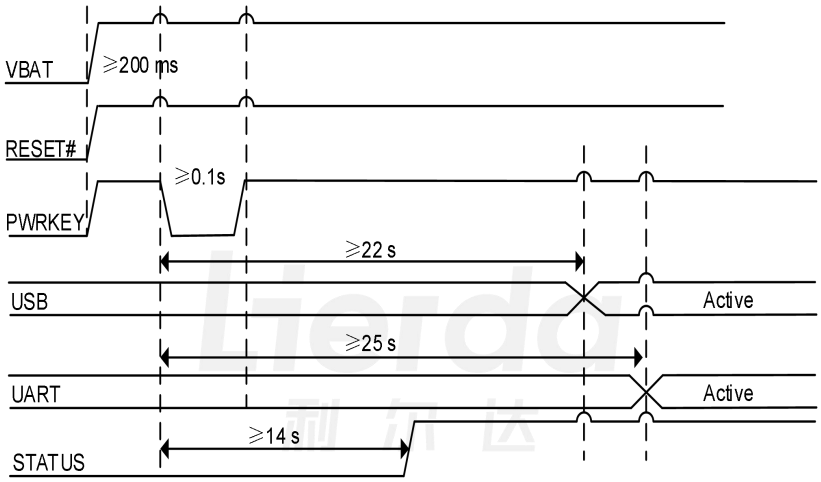


Figure 3.8 Power-on Timing Diagram

Note

- Before pulling down the PWRKEY pin, ensure that the VBAT voltage is stable. It is recommended that the time interval between powering on VBAT and pulling down the PWRKEY pin is not less than 200 ms. The timing here is related to the boot-up process of UART and USB, and in terms of AT commands, the timing difference between the two is not significant.

3.5.2 Shutdown

When the module is in the boot state, the host pulls down the PWRKEY pin for 10 seconds. The module will execute the shutdown process, which takes about 12 seconds.

In addition, you can also power off using the AT+LPOWD command. The command has the same effect as pulling down the PWRKEY to power off.

Shutdown timing sequence is as shown in the figure:

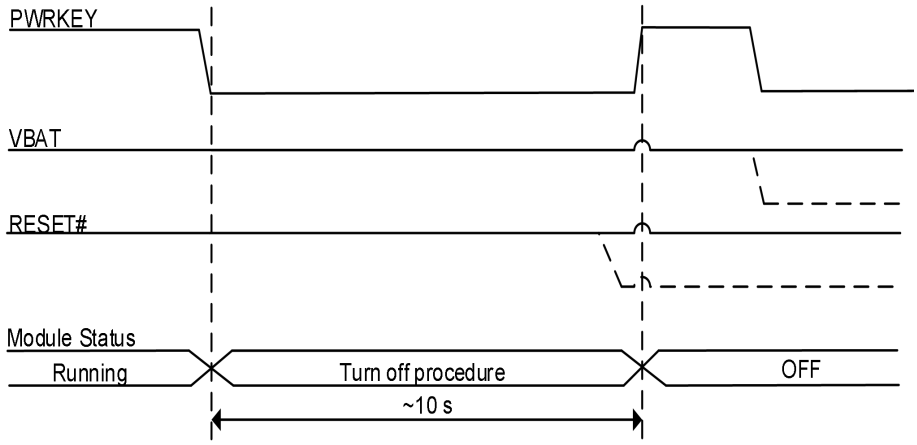


Figure 3.9 Shutdown Timing Diagram

Note

- When the module is working normally, do not cut off the power supply immediately to avoid damaging the Flash inside the module. It is recommended to first turn off the module through PWRKEY or AT+LPOWD, and then disconnect the power supply.
- After the AT command is executed successfully, it will return OK. Afterwards, the UE will activate the network and enter the power-down state by outputting POWER DOWN. The maximum duration for network activation is 60 seconds, and the customer should pay attention to the shutdown time during the design. To avoid data loss, the module must not be powered off before outputting POWER DOWN.

3.6 Reset

The NR90-HEA module can be reset by using the RESET_N pin.

Table 3-7 RESET_N Interface Description

Pin numb	Pin names	Type	Description	Parameter	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
20	RESET_N	DI	Module reset	VIH	1.5	-	1.8	Low-level pulse effective.

Pin numb	Pin names	Type	Description	Parameter	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
				VIL	0	-	0.5	

When the module is powered on, pulling down the RESET_N pin for 100ms or longer can reset the module. The RESET_N signal is sensitive to interference, so it is recommended to keep the traces on the module interface board as short as possible and include GND handling.

Customers can use an open-drain drive circuit or a button to control the RESET# pin, refer to the circuit as shown in the figure below.

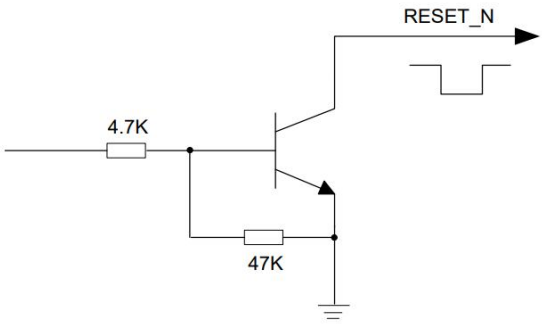


Figure 3.10 Open-Drain Driven Reset Reference Circuit

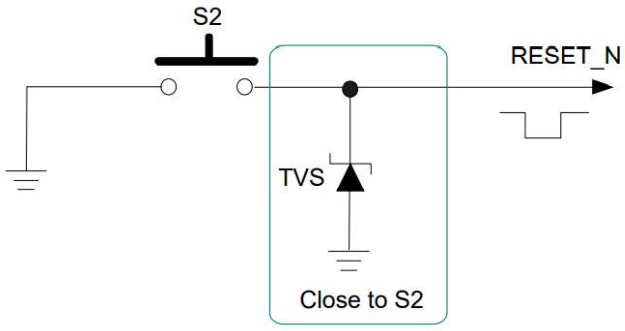


Figure 3.11 Key Reset Reference Circuit

The timing diagram for reset is as follows:

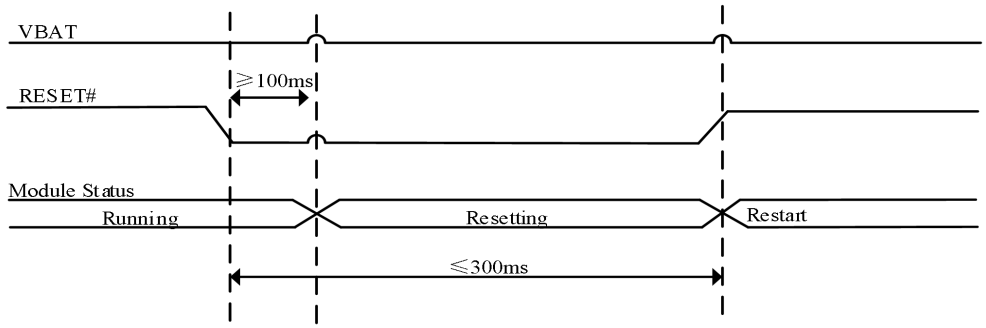


Figure 3.12 Timing Diagram of RESET_N

Note

- Ensure that the maximum load capacitance for the PWRKEY and RESET_N pins does not exceed 47pF.
- The reset function is recommended to be used only after the AT+LPOWD command and PWRKEY shutdown fail.

4 Application interface

This chapter mainly introduces the definition of the NR90-HEA module interface and its related applications.

- UART interface
- USB interface
- PCIe interface
- (U)SIM interface
- I2C interface
- PCM/I2S and SPI interfaces
- ADC interface
- Status indicator interface
- USB_BOOT interface
- RGMII interface
- SDIO interface
- WIFI control interface
- Antenna control interface*
- B code/1PPS timing interface
- LED interface
- GPIO interface
- Antenna interface

4.1 UART interface

The NR90-HEA module has 3 serial ports: main serial port, debug serial port, and GPS serial port. The main features are as follows:

- The main serial port can be used for AT command sending and data transmission, with a default baud rate of 115200bps.
- Debug the serial port for partial log printing, with the default baud rate set to 115200

bps.

- The GPS serial port is used to connect to GPS, AP and other devices, with ordinary serial port function, and the function can be combined with GPIO to achieve.

Table 4-1 Main Serial Port and Flow Control Interface Pin Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
67	MAIN_TXD	DO	Main serial port transmission	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
68	MAIN_RXD	DI	Main serial port reception	VIH	1.26	1.8	1.98	
				VIL	0	-	0.54	
63	MAIN_DCD	DO	Main serial port carrier detection	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
66	MAIN_DTR*	DI	Main serial port receives data. Wake/Sleep Activation	VIH	1.26	1.8	1.98	
				VIL	0	-	0.54	
62	MAIN_RI*	DO	Main serial port ringing prompt	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
64	MAIN_CTS	DO	Clear the sent data	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
65	MAIN_RTS	DI	Request to send data	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
113	GPS_RXD	DI	GPS serial port reception	VIH	1.26	1.8	1.98	
				VIL	0	-	0.54	
114	GPS_TXD	DO	GPS serial port transmission	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	

Table 4-2 Debug Serial Port Interface Pin Description

Pin numb	Pin name	Type	Description	Parameters	Minimum value (V)	Typical Value (V)	Maximum value (V)	Note
11	DBG_RXD	DI	Debugging serial port reception	VIH	1.26	1.8	1.98	If not used, leave floating
				VIL	0	-	0.54	
12	DBG_TXD	DO	Debug serial port transmission	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	

When using the serial port, it is essential to pay attention to the issue of level consistency. The module's serial port level is 1.8V. If you need to connect to different levels such as 3.3V, you need to add a level conversion circuit. Details are as follows:

4.1.1 Transistor level conversion reference circuit

This circuit does not have special requirements for the power supply voltage of the

module, and it is low cost, but it has limitations on the serial port baud rate. The reference design is as follows, also pay attention to the direction of level conversion.

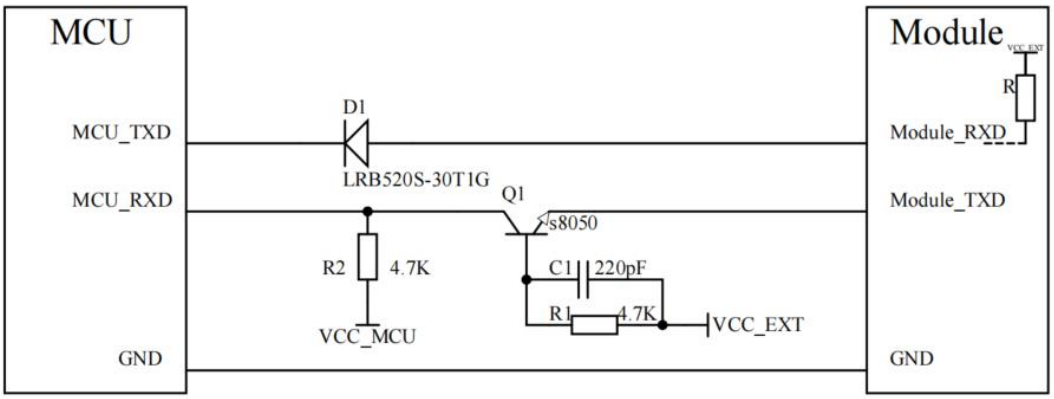


Figure 4.1 Transistor Level Conversion Reference Circuit

Note

- If there is no internal pull-up in the module, the user of the diode conversion circuit needs an external pull-up. The internal pull-up of the NR90-HEA module is up to the 1.8V voltage domain.
- In this circuit, MCU_TXD defaults to outputting 3.3V, and VDD_EXT (LDO8_1V8) defaults to 1.8V. For the diode conversion circuit, it should be noted that the cathode voltage of the diode needs to be higher than the anode voltage in order to achieve the above circuit function.
- This level conversion circuit is not suitable for applications with a baud rate exceeding 460Kbps.

4.1.2 MOSFET level conversion reference circuit

This circuit does not have special requirements for the power supply voltage of the module, and it is low cost, able to meet the requirement of serial port baud rate 921600bps. The reference design is as follows, also pay attention to the direction of level conversion.

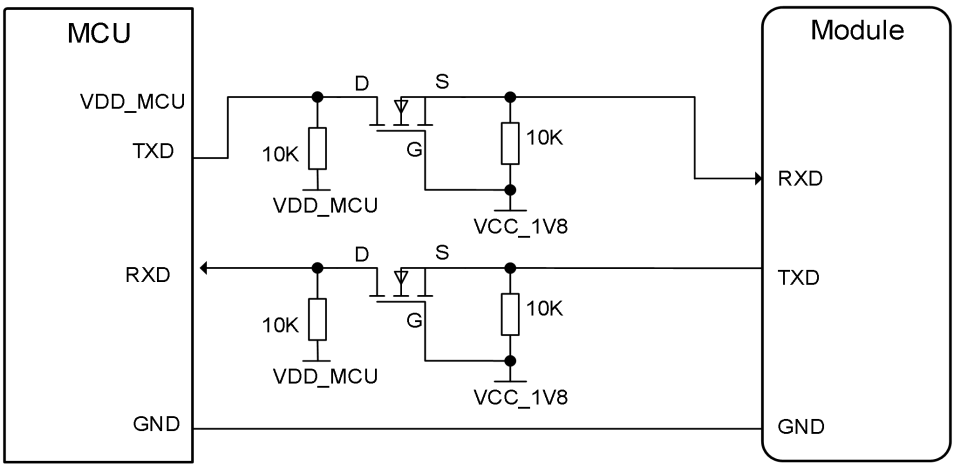


Figure 4.2 Reference Circuit for MOSFET Level Conversion

Recommend MOSFET for reference:

Brand: LRC; Specification model: L2N7002LT1G, the corresponding internal principle is as follows:

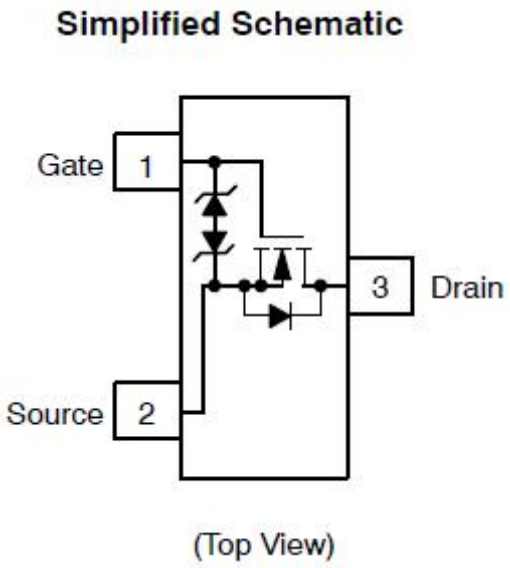


Figure 4.3 MOSFET device diagram

4.1.3 Reference circuit for level conversion chip

This circuit has a slightly higher cost, but with a higher speed, it can meet the typical usage requirements of the serial port. It is recommended to use the TXS0108EPWR from TI company.

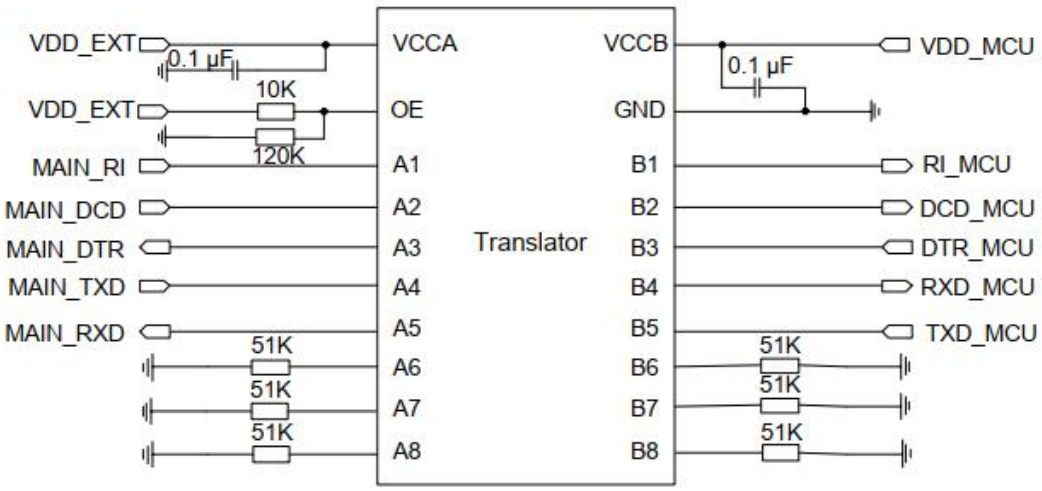


Figure 4.4 Level Conversion Chip Circuit

4.2 USB interface

The NR90-HEA module supports 1 USB interface, which complies with the USB 2.0 specification and supports both high-speed (480Mbps) and full-speed (12Mbps) modes of USB 2.0. The USB interface can be used for AT command transmission, data transfer, software debugging, and firmware upgrades. The table below shows the pin definitions of the USB interface.

Table 4-3 USB Interface Pin Description

Pin number	Pin names	Type	Describe	Note
69	USB_DP	AIO	USB differential data (+)	90Ω differential impedance
70	USB_DM	AIO	USB differential data (-)	
71	USB_VBUS	PI	USB detection	For USB detection only, not for power supply.

USB_VBUS will trigger the power-on, if the module is in the power-off state and USB_VBUS is at a high level, the module will power on. It is recommended to add a USB_VBUS enable or switch circuit.

When designing, it is recommended to reserve test points for the USB 2.0 interface, which can be used for firmware upgrades and debugging. The USB 2.0 reference design

circuit is as follows:

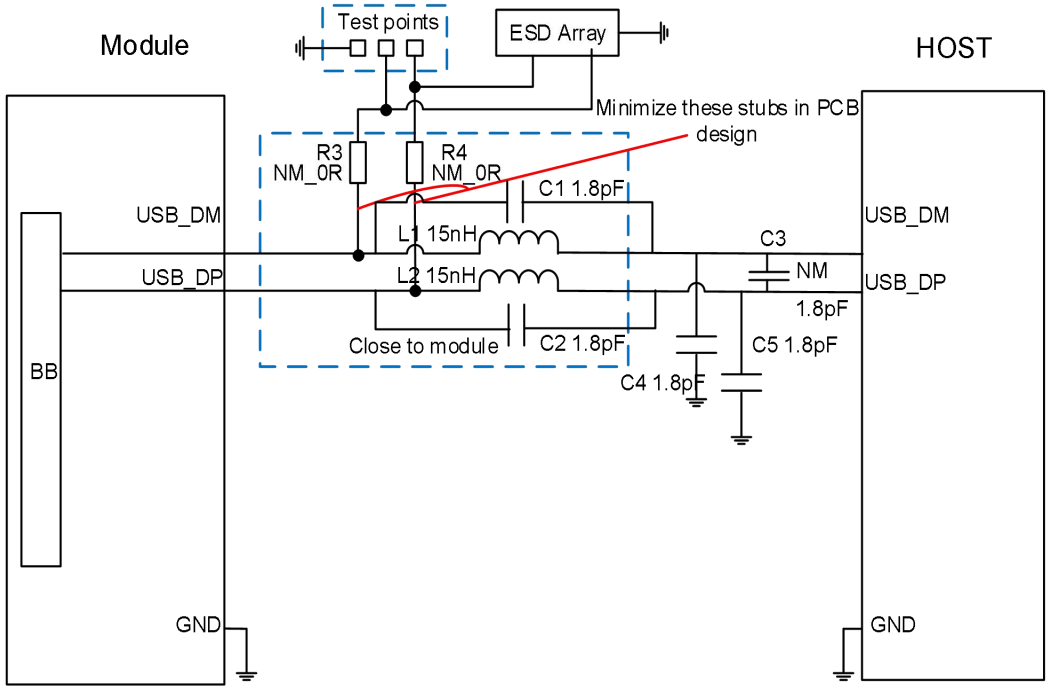


Figure 4.5 USB reference design diagram

The LC trap circuit, placed near the host's USB 2.0 interface, defaults the C3 capacitor at the DP/DM end to NM, and requires the two capacitors to be close to each other.

Note

- In the circuit design of the USB interface, to ensure the performance of USB, the following principles are recommended to be followed in the design: Ground processing is needed around the USB routing, using 90Ω differential impedance lines. Do not route USB lines under crystal oscillators, oscillators, magnetic devices, DC-DC power inductors, and RF signals. It is recommended to use inner layer differential lines and surround them with ground on all sides. When selecting ESD protection devices for USB data lines, pay attention to ensure that the parasitic capacitance of USB 2.0 does not exceed 1pF, and ensure that the signal passes through the ESD protection device first.

4.3 PCIe interface

The NR90-HEA module contains a PCIe interface that complies with PCIe 1.1

specifications and only supports RC mode. For detailed AT command information, please refer to the NR90-HEA AT Command Manual. The main features of the PCIe interface are as follows:

- Support PCIe Gen1 (2.5Gbps max)
- Support PCIe to Ethernet conversion.
- Only support RC mode

Table 4-4 PCIe Interface Pin Description

Pin number	Pin names	Type	Description	Note
126	PCIE_RX_M	AI	PCIe receive data (-)	
127	PCIE_RX_P	AI	PCIe receive data (+)	
138	PCIE_TX_M	AO	PCIe transmits data (-)	
139	PCIE_TX_P	AO	PCIe transmits data (+)	
136	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	RC mode: Output (default)
137	PCIE_REFCLK_P	AIO	PCIE reference clock (+)	
135	WAKE_ON_WIRELESS	DI	PCIe Wake-up	RC mode: Input (default)
124	PCIE_PERST_N	DIO	PCIe reset	RC mode: Output (default)
140	PCIE_CLKREQ_N	OD	PCIe clock request	RC mode: Input (default)

NR90-HEA PCIe interface operates in RC mode, the following diagram shows the reference circuit for NR90-HEA using the PCIe interface to connect devices:

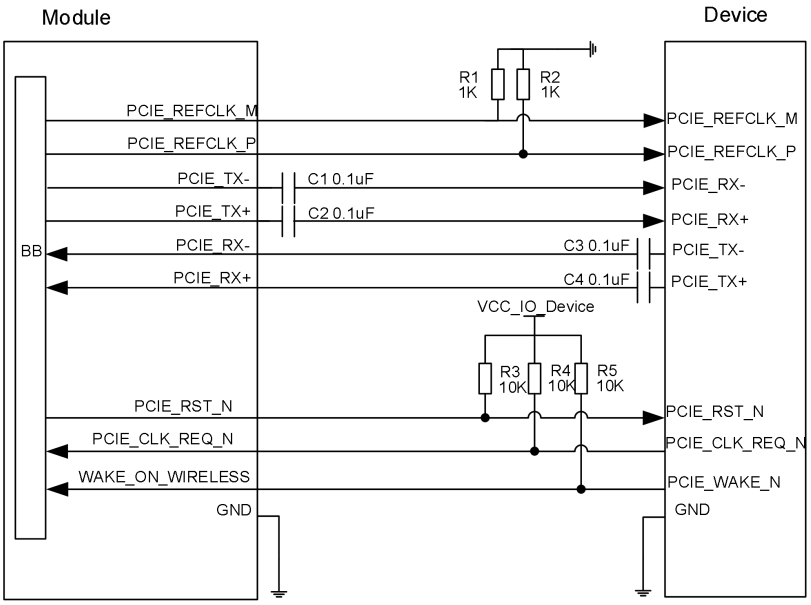


Figure 4.6 Reference Design of Module Connection with PCIe Device (RC Mode)

Note

- Capacitors C1, C2, C3, and C4 should be placed close to the TX PIN, recommended values are 0.1uF, +/-10%, X5R or X7R.
- Resistor R1 and R2 are recommended to be 1K in value.
- CLK, TX, and RX three pairs of differential signal lines need to be routed according to 100Ω +/-10% differential impedance control.
- When routing PCIe, stay away from sensitive signal sources such as RF, audio, and crystal oscillators.
- PCIe traces should not be routed below components and must not cross paths with other signals.
- CLK, TX, and RX should be routed with differential signal lines as short as possible, ideally within 350mm, and maintain a 3W line width between differential pairs and other signals.
- CLK, TX, and RX should be routed in differential pairs with top, bottom, left, right, and three-dimensional grounding.
- When connecting to a host or PC in the 3.3V voltage domain, pay attention to use a voltage conversion chip to maintain level compatibility.

4.4 (U)SIM card interface

4.4.1 (U)SIM pin description

The module supports 1 (U)SIM card interface and hot swapping. Dual SIM single standby function can be achieved through SIM_SWITCH and conversion circuit. The interface complies with ETSI and IMT-2000 card specifications, supporting 1.8V and 3.0V (U)SIM cards. The table below introduces the interface definition of (U)SIM.

Table 4-5 (U)SIM card interface definition

Pin numbe	Pin names	Type	Describe	Parameter	Minimum value (V)	Typical value (V)	Maximum value	Note
17	USIM_RST	DO	(U)SIM card reset	VOH	1.62/2.1	1.8/3.0	1.98/3.3	If not used, leave floating
				VOL	0	-	0.18/0.3	
16	USIM_CLK	DO	(U)SIM card clock	VOH	1.62/2.1	1.8/3.0	1.98/3.3	
				VOL	0	-	0.18/0.3	
15	USIM_DATA	DIO	(U)SIM card data	VIH	1.2/2.1	1.8/3.0	1.98/3.3	
				VIL	0	-	0.54/0.9	
14	USIM_VDD	PO	(U)SIM card	-	1.62	1.8/3.0	3.3	
13	USIM_DET	DI	(U)SIM card detection	VIH	1.26	1.8	1.98	Attention to logic insertion,
				VIL	0	-	0.54	
18	SIM_SWITCH	DO	SIM card switch signal	VIH	1.26	1.8	1.98	Default low level
				VIL	0	-	0.54	

The schematic diagram of the (U)SIM interface circuit design is as follows:

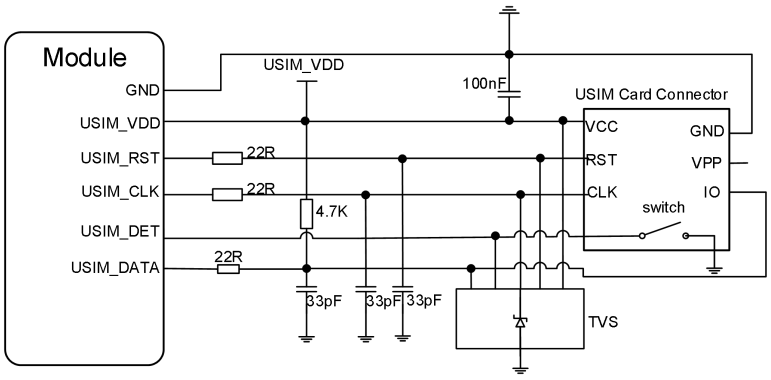


Figure 4.7 8-pin (U)SIM interface reference circuit diagram

The principle of the SIM card slot with detection signal is as follows (design should pay attention to the logic of card insertion). Taking the MUP-C792 card slot connector as an example, the specification sheet describes the Detect Switch as follows,

ELECTRIC FUNCTION	DETECT SWITCH
WITHOUT CARD	CLOSED
CARD INSERTED	OPEN

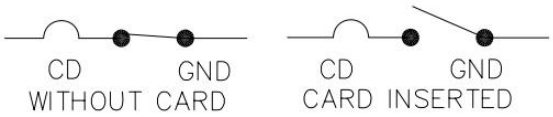


Figure 4.8 SIM card connector Detect Switch operation schematic

When the SIM card is inserted, USIM_DET is at a high level, and when the SIM card is removed, USIM_DET is at a low level.

If the USIM card detection function is not required, please leave the USIM_DET pin floating. The following is the 6-pin USIM interface reference circuit:

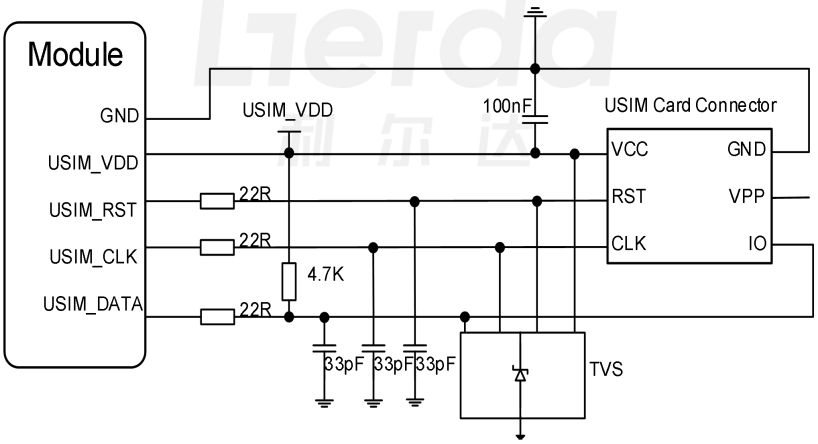


Figure 4.9 6-pin (U)SIM interface reference circuit diagram

Dual SIM single standby solution can be achieved through SIM_SWITCH and switch circuit. The main chip supports one SIM card interface externally,

The switching between dual SIM cards can be achieved through an external switch, including the signal pins and power supply of the SIM cards.

Regarding hot swap mode, the system supports simulating switch toggling of SIM_SW and SIM_DET pins, Lierda NR90-HEA module is supported.

SIM card quick power off. Dual card single standby reference diagram as shown in the following figure.

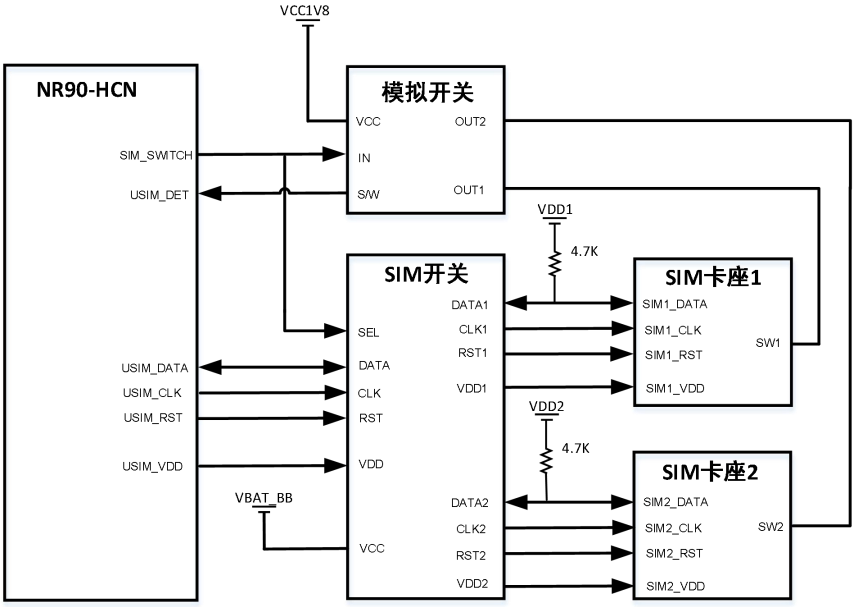


Figure 4.10 Reference Diagram for SIM Dual Card Single Standby Solution

4.4.2 Hot-swappable (U)SIM

The NR90-HEA module supports (U)SIM card hot-swapping function by detecting the USIM_DET pin status of the (U)SIM card slot to determine the insertion and removal of the (U)SIM card, thereby supporting the (U)SIM card hot-swapping function. The (U)SIM card hot-swapping function can be configured using the AT+LSIMDET command.

Table 4-6 USIM_DET Control Voltage Description

AT format	AT command	SIM card hot plug detection	Function Description
Read Command AT+LSIMSTAT? Write Command AT+LSIMSTAT=<enable>,<insert_level>	AT+LSIMDET=1,0	Start	The (U)SIM card hot-plug detection function is enabled, and the module detects whether the (U)SIM card is inserted through the USIM_DET pin status detection, with low-level detection.

	AT+LSIM DET=1,1	Start	The (U)SIM card hot plug detection function is enabled, and the module detects whether the (U)SIM card is inserted through the USIM_DET pin status detection, detecting a high level.
	AT+LSIM DET=0,0 AT+LSIM DET=0,1	Close	SIM card hot swap detection function disabled, module reads (U)SIM card on boot without checking USIM_DET status

Note

- NR90-HEA module (U)SIM card hot swap function is disabled by default.
- If hot swap is enabled, the <insert_level> value must match the insertion level designed in the hardware, otherwise the hot swap function will be invalid.
- If a (U)SIM card has been successfully detected, the command to control the (U)SIM card detection function is no longer supported. The command to control the (U)SIM card detection function can only be used again after the module is restarted or the (U)SIM card is hot-swapped.

4.4.3 Requirements for (U)SIM card interface design

In the circuit design of the (U)SIM card interface, in order to ensure the good functional performance of the (U)SIM card and prevent damage, the following design principles are recommended to be followed in the circuit design:

- The distance between the (U)SIM card holder and the module bracket should not be too far, the closer the better, try to ensure that the (U)SIM card signal line wiring does not exceed 200mm.
- (U)SIM card signal line wiring should be kept away from RF lines and VBAT power lines.
- To prevent possible crosstalk from the USIM_CLK signal to the USIM_DATA signal, they should not be wired too close together. Ground shielding should be added between the two traces, and ground protection is also needed for the USIM_RST signal.

- To ensure good ESD protection, it is recommended to add TVS diodes placed close to the (U)SIM card holder. The parasitic capacitance of the selected ESD device should not exceed 10pF. A 0-ohm resistor can also be placed in series between the module and (U)SIM card for debugging purposes. 33pF capacitors can be connected in parallel on the USIM_DATA, USIM_CLK, and USIM_RST lines to filter out RF interference. Peripheral components of the (U)SIM card holder should be placed as close as possible to the (U)SIM card holder.
- Adding a pull-up resistor to USIM_DATA can enhance the anti-interference capability of the (U)SIM card, it is recommended to reserve a pull-up resistor near the (U)SIM card slot.

4.5 I2C interface

The NR90-HEA module provides a set of I2C interfaces, supporting standard and fast modes.

Table 4-7 I2C Interface Description

Pin number	Pin names	Type	Describe	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
41	I2C_SCL	OD	I2C clock signal	VIH	1.17	1.8	1.98	If not used, leave floating
				VIL	-0.3	-	0.63	
				VOH	1.35	1.8	1.98	
				VOL	-0.3	-	0.45	
42	I2C_SDA	OD	I2C data signal	VIH	1.17	1.8	1.98	If not used, leave floating
				VIL	-0.3	-	0.63	
				VOH	1.35	1.8	1.98	
				VOL	-0.3	-	0.45	

The I2C interface schematic diagram is as shown in the following figure, and attention should be paid to level matching when designing the principle:

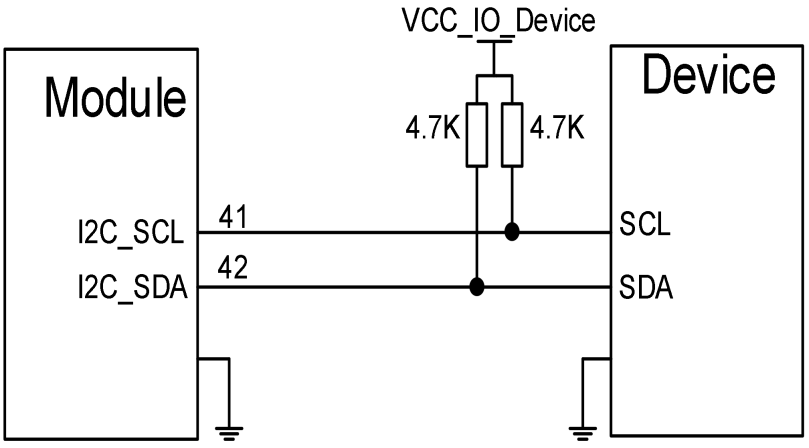


Figure 4.11 I2C Reference Design

Note

Adjust the resistance value of the pull-up resistor to 4.7K according to the actual usage

scenario.

4.6 PCM and SPI interfaces

The NR90-HEA module has one group of PCM (I2S) interface. It supports external Codec chip via PCM and I2C interface, or external SLIC via PCM and SPI interface.

Table 4-8 PCM (I2S) and SPI Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
24	PCM_IN	DI	PCM data input	VIH	1.26	1.8	1.98	If not used, leave floating
				VIL	0	-	0.54	
25	PCM_OUT	DO	PCM data output	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
26	PCM_SYNC	DO	PCM synchronous output	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
27	PCM_CLK	DO	PCM clock output	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
				VOL	0	-	0.18	
37	SPI_CS_N	DO	SPI chip select	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
39	SPI_MISO	DI	SPI input	VIH	1.26	1.8	1.98	
				VIL	0	-	0.54	
40	SPI_CLK	DO	SPI clock	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
38	SPI_MOSI	DO	SPI output	VOH	1.62	1.8	1.98	
				VOL	0	-	0.18	
				VIL	0	-	0.54	

The external Codec device schematic diagram is as shown in the following figure, detailed design can be found in the NR90-HEA module reference design:

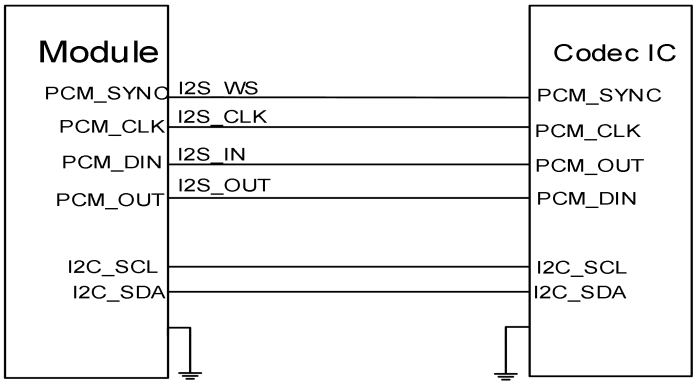


Figure 4.12 PCM/I2S External Codec Reference Design

The external SLIC device schematic is shown in the following figure, detailed design can be found in the NR90-HEA module reference design:

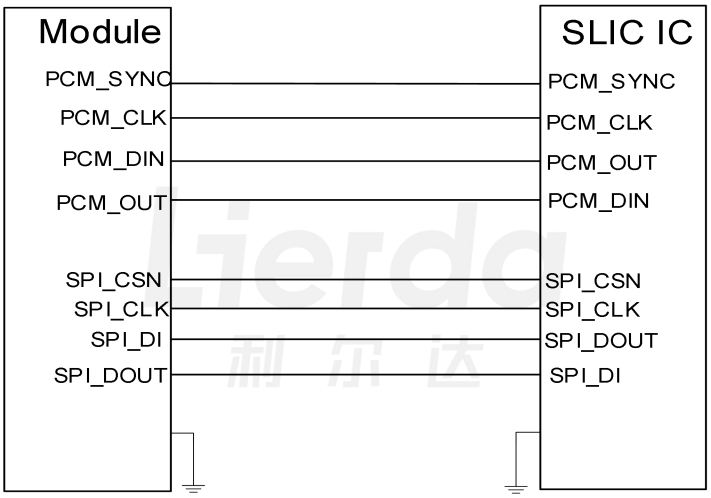


Figure 4.13 Reference Design for PCM and SPI External SLIC

Note

- Detailed connection of Codec or SLIC circuit can be found in the "NR90-HEA Hardware Reference Design Manual".

4.7 ADC interface

The NR90-HEA module provides 2 channels of analog-to-digital conversion output interfaces. To ensure the accuracy of ADC voltage detection, grounding treatment is required in wiring. The ADC sampling accuracy is 12 bits.

Table 4-9 ADC Interface Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value	Note
44	ADC1	AI	ADC0	Voltage range	0	-	1.75	If not used, leave floating
45	ADC0	AI	ADC1	Voltage Range	0	-	1.75	

Note:

- The ADC sampling accuracy is 12 bits.
- ADC input voltage must not exceed 1.75V, otherwise the module will be damaged.

4.8 Status indicator interface

4.8.1 Network status indicator

The NR90-HEA module indicates the network status of the module through the NET_MODE and NET_STATUS pins, as shown in the table below.

Table 4-10 Network Status Indicator Pin Description

Pin number	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Notes
5	NET_MODE	DO	Registration network mode indication	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
6	NET_STATUS	DO	Network status indicator	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	

Table 4-11 Network Status Indicator Description

Pin names	Pin working status	Network Status
NET_MODE	High level	Register network status
	Low level	Other

Pin names	Pin working status	Network Status
NET_STATUS*	Slow flash (200 ms high/1800 ms low)	Check network status
	Slow Flash (1800 ms high/200 ms low)	Standby mode
	Quick Flash (125 ms high/125 ms low)	Data transmission mode
	High Level	During the call

Reference circuit as follows:

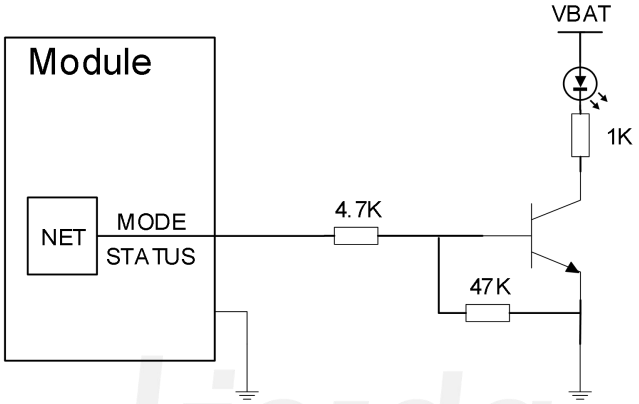


Figure 4.14 Network status indicator reference circuit

4.8.2 Module running status indicator

The NR90-HEA module indicates whether the module is in normal operation through the STATUS pin, as shown in the table below.

Table 4-12 Explanation of STATUS Working Status

Pin names	Pin working status	Network status
STATUS	High level	Other
	Low level	The module is operating normally.

NR90-HEA module supports 1 channel LED SINK pin, LED driving is achieved through this pin, and this pin allows a maximum input current of 20mA. The reference circuit is as follows:

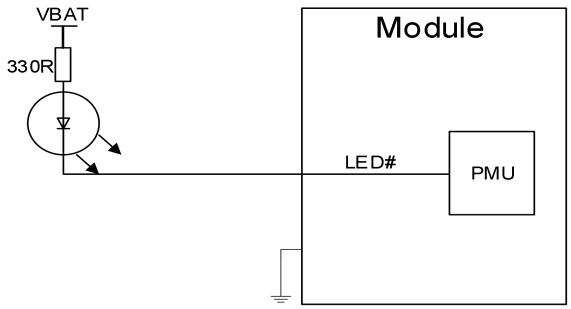


Figure 4.15 LED interface reference circuit

4.8.3 MAIN_RI*

MAIN_RI can have multiple indication methods as a signaling signal, the default indication methods are as follows:

Table 4-13 Explanation of MAIN_RI Indication Status

Pin names	Pin working status	Network Status
MAIN_RI*	High level	Idle
	Low level	When the new URC returns, MAIN_RI will have a low level of 1S.

4.9 USB_BOOT interface

The NR90-HEA module supports USB_BOOT function, which means grounding the USB_BOOT before powering on to enable the module to enter emergency download mode. In the download mode, the module firmware can be upgraded via USB 2.0.

Table 4-14 USB_BOOT Interface Description

Pin numb	Pin Name	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
115	USB_BOOT	DI	Emergency download mode	VIH	1.26	1.8	1.98	If not used, leave floating
				VIL	0	-	0.54	

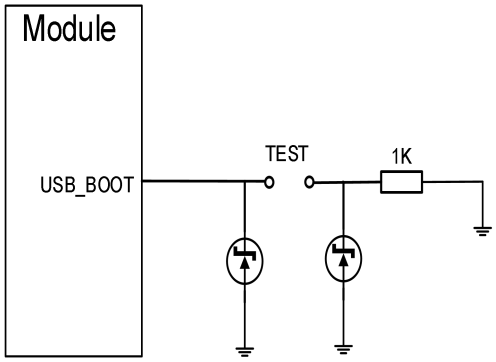


Figure 4.16 USB_BOOT Interface Reference Circuit

4.10 RGMII interface

The NR90-HEA module provides a set of RGMII interfaces for connecting to Ethernet PHY/MAC. Below are the interface description and design requirements for the RGMII interface.

Table 4-15 RGMII Interface Description

Pin numbe	Pin name	Type	Description	Parameter	Minimum value	Typical value	Maximum value	Note
73	RGMII_RX_D1	DI	RGMII receive data1	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.3	
74	RGMII_RX_EN	DI	RGMII receive control	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.3	
75	RGMII_RX_CLK	DI	RGMII receive clock	VIH	1.62	1.8	1.98	If not used, leave floating
				VIL	-0.3	-	0.3	
76	RGMII_RX_D0	DI	RGMII receives data 0	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.3	
77	RGMII_TX_D0	DO	RGMII sends data 0	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.3	
78	RGMII_TX_D1	DO	RGMII transmits data 1	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.3	
79	RGMII_RX_D2	DI	RGMII receive data 2	VOH	1.62	1.8	1.98	If not used, leave
				VOL	-0.3	-	0.3	

Pin numbe	Pin name	Type	Description	Parameter	Minimum value	Typical value	Maximum value	Note
								floating
80	RGMII_TX_D2	DO	RGMII send data 2	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	If not used, leave floating
81	RGMII_TX_EN	DO	RGMII transmission control	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	If not used, leave floating
82	RGMII_RX_D3	DI	RGMII receive data 3	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	If not used, leave floating
83	RGMII_TX_CLK	DO	RGMII transmit clock	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	If not used, leave floating
84	RGMII_TX_D3	DO	RGMII sends data 3	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	If not used, leave floating
119	RGMII_RST_N	DO	PHY device reset signal	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	1.8V power domain
120	EPHY_INT_N	DI	Interrupt signal in PHY devices	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	1.8V power domain
121	RGMII_MDIO	OD	MDI24 Interface Data Input/Output Signal	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	1.8V power domain
122	RGMII_MDC	DO	MDI24 interface clock output	VOH VOL	1.62 -0.3	1.8 -	1.98 0.3	1.8V power domain

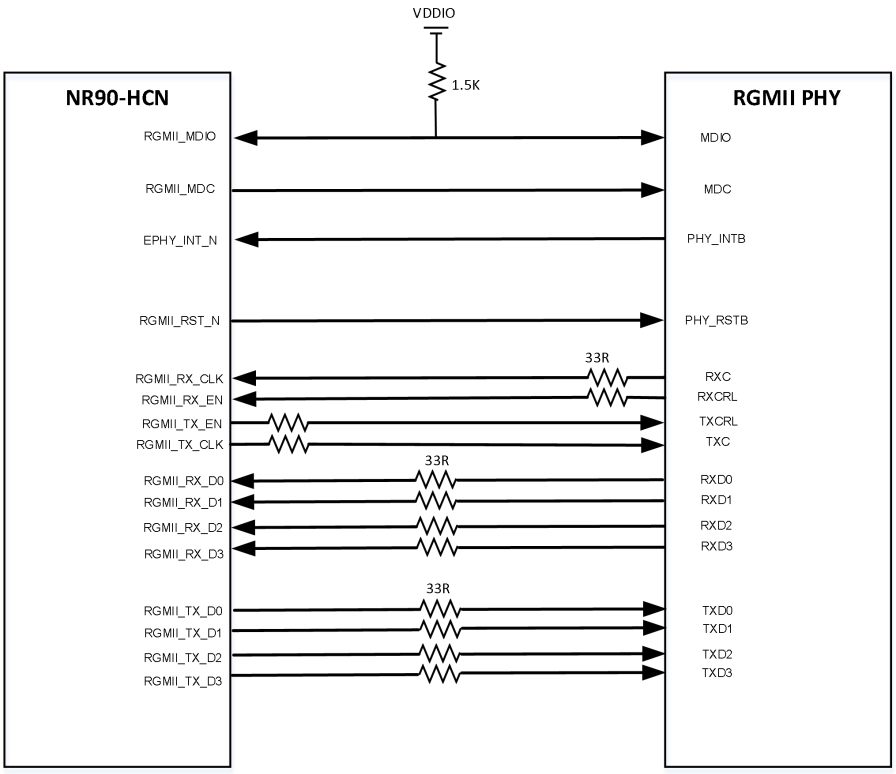


Figure 4.17 RGMII Interface Reference Circuit

Note

- Require RGMII routing to be single-ended with 50Ω impedance control, and try to use inner layer vias as much as possible to reduce radiation.
- Supports 10/100/1000Mbps rates, corresponding TX/RX CLK frequencies are 2.5/25/125 MHz.
- To ensure good EMI performance, the RGMII clock/data routing should be less than 15cm.
- RGMII related signals are susceptible to interference and require a solid GND plane for protection. Try to keep away from power sources/crystals/RF/switch signals, etc.
- TX_CLK/RX_CLK are high-speed clock signals, it is recommended to maintain a 10 mil spacing between the clock and data signals.
- To avoid the parasitic capacitance caused by the reflection of the signal at a 90-degree angle, it is recommended to use a 45-degree corner for routing.
- RX/TX needs to be routed in separate groups, with the internal lengths controlled

within ±100 mil.

- Try to keep RGMII traces away from nearby heat sources. Stay at least 20 mil away from I/O signals.

4.11 SDIO interface

The NR90-HEA module provides an SDIO interface for connecting to WIFI devices, supporting SDIO Version 3.0 protocol commands, and Bus Speed Modes supporting SDR12, SDR25, SDR50. The module's SDIO can only function as a Master and does not support Slave mode.

Table 4-16 SDIO Interface Description

Pin numb	Pin names	Type	Describe	Parameters	Minimum value	Typical value	Maximum	Note
28	SDC_DATA3	DIO	SDIO bus DATA3	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
29	SDC_DATA2	DIO	SDIO bus DATA2	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
30	SDC_DATA1	DIO	SDIO bus DATA1	VIH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
31	SDC_DATA0	DIO	SDIO bus DATA0	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
32	SDC_CLK	DO	SDIO bus clock	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
33	SDC_CMD	DIO	SDIO bus clock	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	

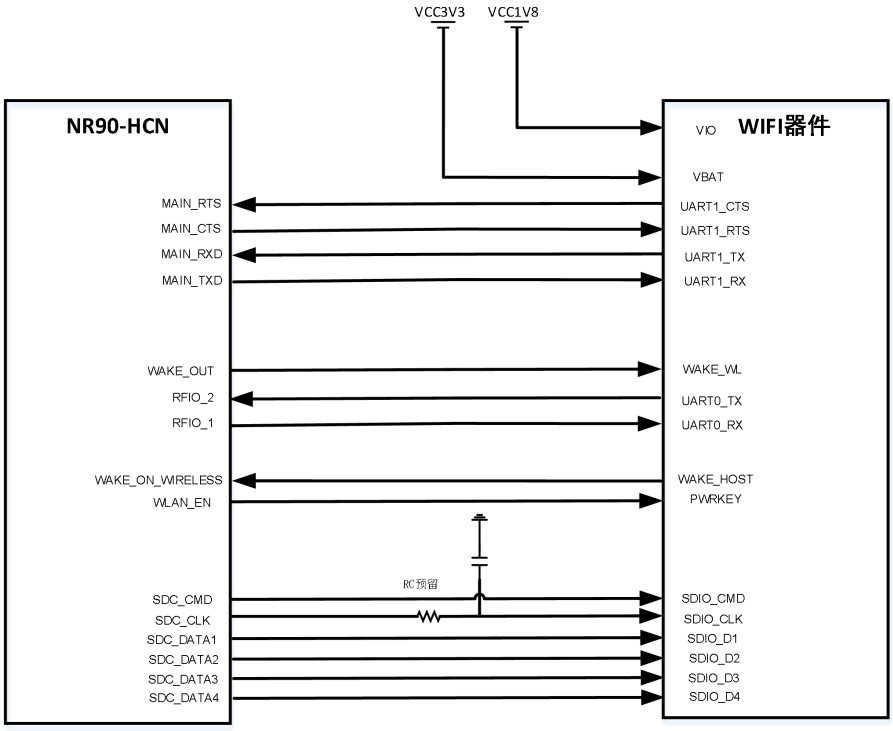


Figure 4.18 SDIO interface docking WIFI reference circuit

4.12 WIFI control interface

The module reserves 2 WIFI control interfaces to achieve low-cost WIFI usage. The 32K is closed by default, and the RFIO function is under development. If the function needs to be used, please contact our FAE.

Table 4-17 WIFI Control Interface Description

Pin numb	Pin names	Type	Description	Parameters	Minimum value	Typical value	Maximum	Note
118	WLAN_SLP_32K	AO	WLAN sleep clock	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
125	WLAN_EN	DO	WIFI enable	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	
143	RFIO_1	DIO	Antenna tuning switch control	VIH	1.62	1.8	1.98	If not used, leave floating
				VIL	0	-	0.18	
144	RFIO_2	DIO	Antenna tuning switch control	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	

4.13 B code/1PPS timing interface

The NR90-HEA module provides 1 B-code time synchronization interface and 1 1PPS time synchronization interface for external device time synchronization.

Table 4-18 Timing Interface Description

Pin numbe	Pin names	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
3	B_CODE	DO	B code output	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	
116	1PPS_OUT	DO	1PPS output	VOH	1.35	1.8	1.98	If not used, leave floating
				VOL	-0.3	-	0.45	

The following is the reference circuit of the B code output interface:

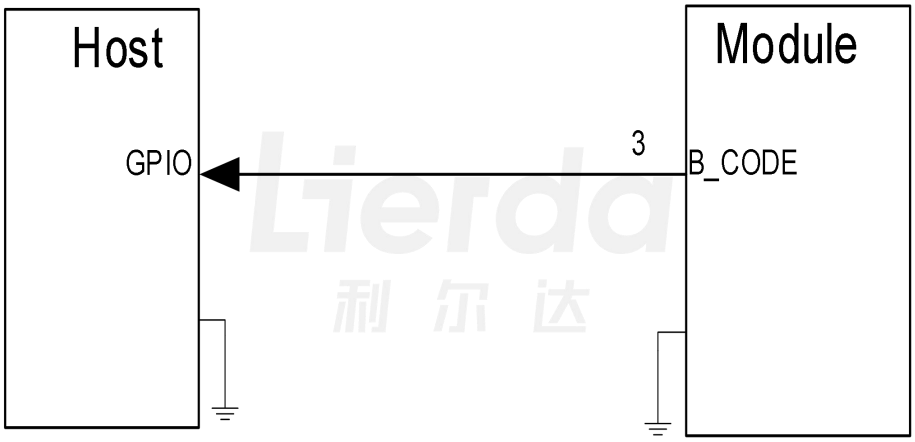


Figure 4.19 Reference Circuit for B Code Output Interface

The following is the reference circuit for the 1PPS output interface:

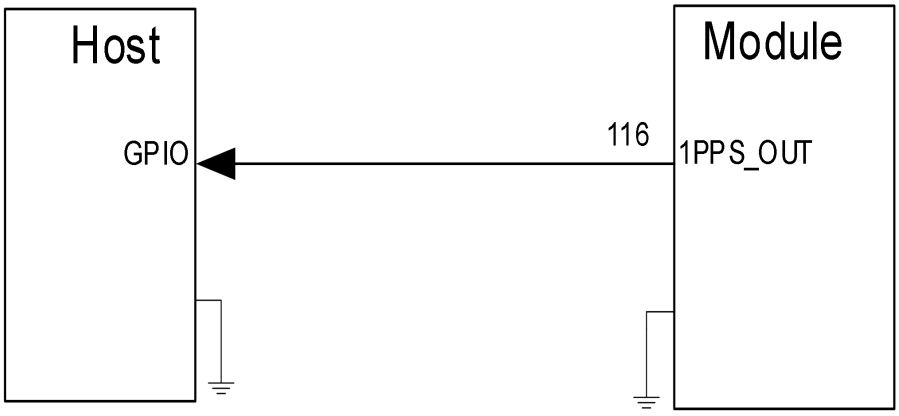


Figure 4.20 1PPS Output Interface Reference Circuit

4.14 GPIO interface

NR90-HEA module reserves 1 general-purpose GPIO pin for expansion, the pin list is as follows, for specific usage please consult our FAE.

Table 4-19 GPIO Interface Description

Pin numbe	Pin name	Type	Description	Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Note
23	GPIO_01	IO	Universal IO control	VOH	1.62	1.8	1.98	If not used, leave floating
				VOL	0	-	0.18	

4.15 Antenna Interface

The NR90-HEA module design has 2 antennas, and their positions and interface definitions are as follows.

4.15.1 Pin Description

Table 4-20 Antenna Interface Pin Definitions

Pins	Antenna	Antenna Types	Frequency band	Frequency Range
49	M	TRx0	**WCDMA:**B1/5/8 **LTE**:B1/3/5/7/8/20/28/38/40/41/42/43 **NR**: n1/3/5/7/8/20/28/41/77/78	703～5000
35	D	Rx1	**WCDMA:**B1/5/8 **LTE**: B1/3/5/7/8/20/28/38/40/41/42/43 **NR**: n1/3/5/7/8/20/28/40/41/77/78	703～5000

When in use, the antenna can be directly led out from the antenna interface of the module, or it can be transferred through the PCB board. When transferring, the RF traces on the board should be as short as possible, and Π-type/double L matching circuits should be reserved for debugging to ensure that the trace impedance is 50Ω.

4.15.2 Antenna reference circuit

The connection reference circuit for ANT_MAIN and ANT_DIV antennas is shown in

the figure below. The routing should be as short as possible, with at least a Π-type matching circuit reserved for debugging, ensuring that the routing impedance is 50Ω.

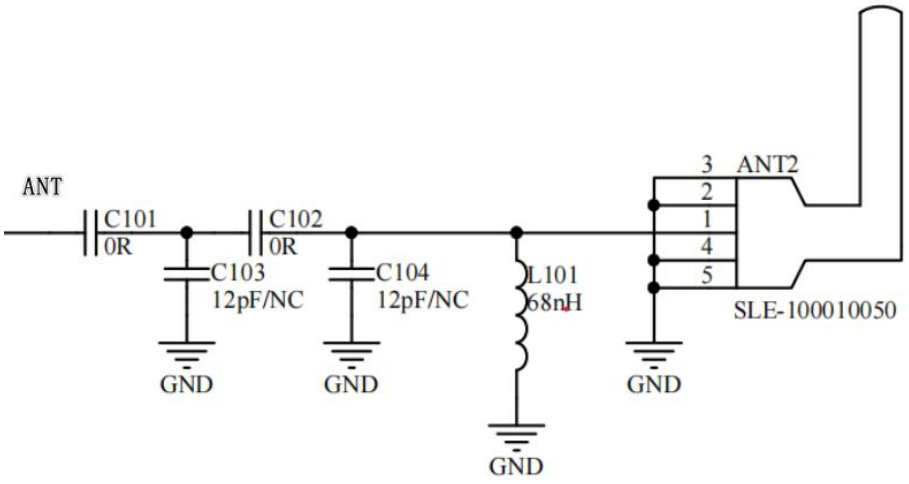


Figure 4.21 Antenna Matching Circuit

4.15.3 RF connector dimensions

The module antenna connector dimensions are as shown in the following figure:

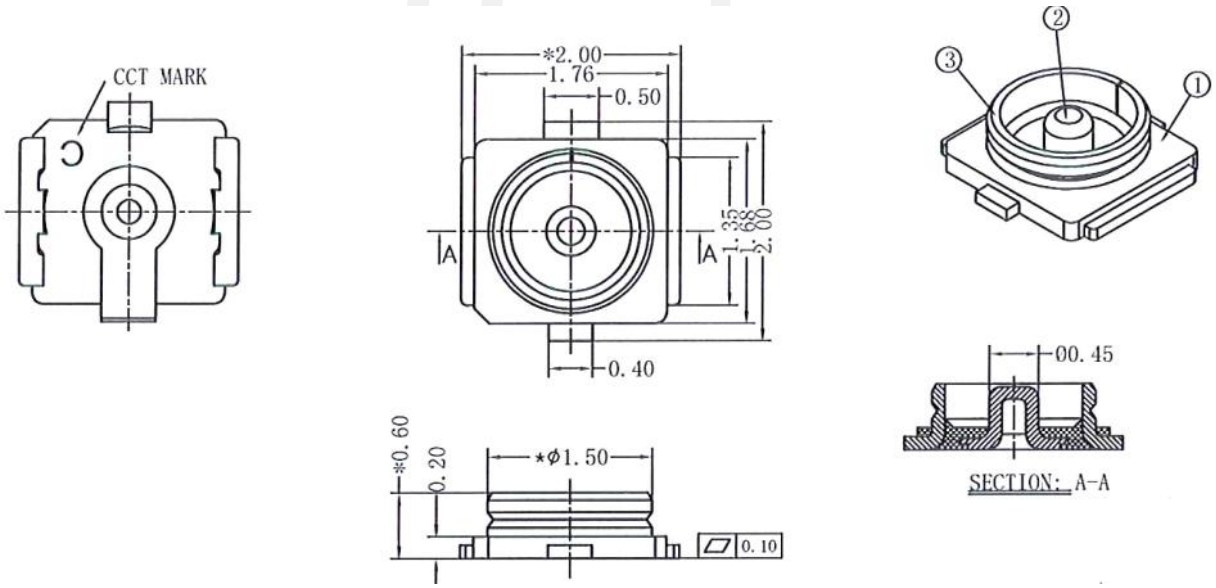


Figure 4.22 Motherboard RF Connector Dimension Diagram (unit: mm)

Table 4-21 Main Characteristics of RF Connectors

Parameters	Standard
Nominal frequency range	DC~6GHz
Characteristic impedance	50Ω

Temperature range	-40~90℃
Voltage Standing Wave Ratio (VSWR)	Maximum 1.3 (0~3 GHz); Maximum 1.4 (3~6 GHz)

4.15.4 RF coaxial cable requirements

The selection of coaxial cables matching the RF connector should refer to the following specifications.

Table 4-22 RF Coaxial Cable Characteristics

Parameters	Standard
Nominal frequency range	DC~6GHz
Line loss	0.1dBm/V@100MHz
Characteristic impedance	50Ω
Temperature range	-40~85℃
Voltage Standing Wave Ratio (VSWR)	Maximum 1.3 (0~3 GHz); Maximum 1.4 (3~6 GHz)

The figure shows the states after the 0.81 fourth-generation end buckle is closed and the 1.13 fourth-generation end buckle is closed.

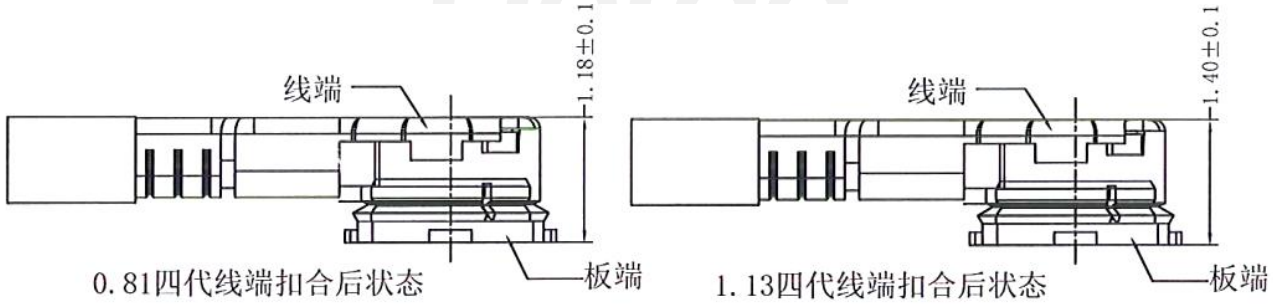


Figure 4.23 The state after the cable line ends are fastened.

4.15.5 Antenna selection requirements

The passive parameters selection of the antenna are as follows.

Table 4-23 Antenna Selection Parameters

Parameters	Standard
Frequency Range	700-5000MHz
Characteristic impedance	50Ω
Standing wave ratio	≤ 2

Efficiency	> 30%
Joint	SMA

Passive parameters are for reference only, actual selection should be based on OTA data.

5 Radio Frequency Characteristics

This chapter mainly introduces the RF characteristics of the module:

- Conduction reception sensitivity
- Transmitting power

5.1 Conduction test data

5.1.1 Test environment

Test equipment: Lierda CMW500, MT8000A

Power: 66319D

5.1.2 Conduction reception sensitivity

The reception sensitivity index is an important parameter for evaluating the performance of the NR90-HEA module, and the test results are shown in the table below.

Table 5-1 Description of Reception Sensitivity

Frequency band	Test value (unit: dBm)			3GPP(SIMO)
	Main Collection	Episode	SIMO	
WCDMA Band 1	TBD	TBD	TBD	-106.7
WCDMA Band 5	TBD	TBD	TBD	-104.7
WCDMA Band 8	TBD	TBD	TBD	-103.8
LTE Band 1(10 MHz)	TBD	TBD	TBD	-96.3
LTE Band 3(10 MHz)	TBD	TBD	TBD	-93.3
LTE Band 5(10 MHz)	TBD	TBD	TBD	-94.3
LTE Band 7(10 MHz)	TBD	TBD	TBD	-93.3
LTE Band 8(10 MHz)	TBD	TBD	TBD	-96.3
LTE Band 20(10 MHz)	TBD	TBD	TBD	-96.3
LTE Band 28(10 MHz)	TBD	TBD	TBD	-96.3
LTE Band 38(10 MHz)	TBD	TBD	TBD	-96.3
LTE Band 40(10 MHz)	TBD	TBD	TBD	-96.3
LTE Band 41(10 MHz)	TBD	TBD	TBD	-94.3
LTE Band 42(10 MHz)	TBD	TBD	TBD	-92.3
LTE Band 43(10 MHz)	TBD	TBD	TBD	-92.3
NR n1(20 MHz)	TBD	TBD	TBD	-93.8

Frequency band	Test value (unit: dBm)			3GPP(SIMO)
	Main Collection	Episode	SIMO	
NR n3(20 MHz)	TBD	TBD	TBD	-90.8
NR n5(10 MHz)	TBD	TBD	TBD	-90.8
NR n7(20 MHz)	TBD	TBD	TBD	-90
NR n8(10 MHz)	TBD	TBD	TBD	-90
NR n20(20 MHz)	TBD	TBD	TBD	-90.8
NR n28(20 MHz)	TBD	TBD	TBD	-92
NR n40(20 MHz)	TBD	TBD	TBD	-92.9
NR n41(20 MHz)	TBD	TBD	TBD	-92.9
NR n77(20 MHz)	TBD	TBD	TBD	-92.9
NR n78(20 MHz)	TBD	TBD	TBD	-92.9

5.1.3 Transmitting power

Transmit power is an important indicator for measuring the performance of the NR90-HEA module, and the test results are shown in the table below.

Table 5-2 Power Transmission Description

Frequency band	Measurement value	3GPP
WCDMA B1	23	24dBm +1.7/-3.7dB
WCDMA B5	23	24dBm +1.7/-3.7dB
WCDMA B8	23	24dBm +1.7/-3.7dB
LTE B1	22	23dBm ±2.7dB
LTE B3	22	23dBm ±2.7dB
LTE B5	23	23dBm ±2.7dB
LTE B7	22.5	23dBm ±2.7dB
LTE B8	23	23dBm ±2.7dB
LTE B20	23	23dBm ±2.7dB
LTE B28	23	23dBm ±2.7dB
LTE B38	23	23dBm ±2.7dB
LTE B40	23	23dBm ±2.7dB
LTE B41	23	23dBm ±2.7dB
LTE B41	25.5	26dBm +2.7/-3.7dB(Class 2)
LTE B42	23	23dBm ±2.7dB
LTE B43	23	23dBm ±2.7dB

Frequency band	Measurement value	3GPP
NR n1	22	23dBm ±2.7dB(Class 3)
NR n3	22	23dBm ±2.7dB(Class 3)
NR n5	23	23dBm ±2.7dB(Class 3)
NR n7	22.5	23dBm ±2.7dB(Class 3)
NR n8	23	23dBm ±2.7dB(Class 3)
NR n20	23	23dBm +2.7/-3.2dB(Class 3)
NR n28	23	23dBm +2.7/-3.2dB(Class 3)
NR n40	23	23dBm +2.7/-3.2dB(Class 3)
NR n41	23	23dBm +2.7/-3.2dB(Class 3)
NR n77	23	23dBm +2.7/-3.2dB(Class 3)
NR n78	23	23dBm +2.7/-3.7dB(Class 3)

6 Electrical performance and reliability

This chapter mainly introduces the electrical characteristics and reliability characteristics of the NR90-HEA module interface.

6.1 Work and storage environment

The operating and storage temperature ranges of the NR90-HEA module are as shown in the table below.

Table 6-1 Working and Storage Temperatures

Parameters	Minimum value (°C)	Maximum value (°C)
Normal operating temperature	-10	+55
Expand working temperature	-40	+85
Storage temperature	-40	+90

6.2 Rated power value

The input voltage requirements for the NR90-HEA module are as shown in the table below.

Table 6-2 Operating Voltage

Parameters	Minimum value (V)	Typical value (V)	Maximum value (V)	Ripple (V)
VBAT_BB	3.3	3.8	4.4	≤0.1
VBAT_RF	3.3	3.8	4.4	≤0.1

6.3 Absolute maximum rated value

Table 6-3 Absolute Maximum Ratings

Parameters	Minimum value (V)	Maximum value (V)
VBAT	-0.3	5.0
Digital Interface Voltage	-0.3	1.98

6.4 Power consumption characteristics

Table 6-4 Power Consumption of the Module

Module status	Condition	Average

		Typ.Current(mA)@ 3.8V
Shutdown mode	Module power off	TBD
Flight Sleep Mode	Flight & Hibernate	TBD
Idle mode	WCDMA @ DRX = 0.64s (USB disconnected)	TBD
	LTE-FDD @ DRX = 0.64s (USB disconnected)	TBD
	LTE-TDD @ DRX = 0.64s (USB Disconnection)	TBD
	NR-FDD @ DRX = 1.28s (USB disconnected)	TBD
	NR-TDD @ DRX = 1.28s (USB disconnected)	TBD
Maximum transmission power of WCDMA	WCDMA B1	TBD
	WCDMA B5	TBD
	WCDMA B8	TBD
Maximum transmission power of LTE	LTE-FDD B1	TBD
	LTE-FDD B3	TBD
	LTE-FDD B5	TBD
	LTE-FDD B7	TBD
	LTE-FDD B8	TBD
	LTE-FDD B20	TBD
	LTE-TDD B28	TBD
	LTE-TDD B38	TBD
	LTE-TDD B40	TBD
	LTE-TDD B41（PC2）	TBD
	LTE-TDD B41（PC3）	TBD
	LTE-TDD B42	TBD
	LTE-TDD B43	TBD
Maximum transmission power of 5G NR	5G NR-FDD n1	TBD
	5G NR-FDD n3	TBD
	5G NR-FDD n5	TBD
	5G NR-FDD n7	TBD
	5G NR-FDD n8	TBD
	5G NR-TDD n20（PC3）	TBD
	5G NR-TDD n28（PC3）	TBD
	5G NR-TDD n40（PC3）	TBD
	5G NR-TDD n41（PC3）	TBD
	5G NR-TDD n77（PC3）	TBD
	5G NR-TDD n78（PC3）	TBD

6.5 ESD protection

6.5.1 ESD design recommendations

The overall ESD performance is mainly determined by: structural shielding, PCB layout protection, and device protection performance. Here are some considerations for device selection:

- Reverse leakage current IR: Excessive reverse current not only increases system power consumption but may also affect signal functionality, especially noticeable in high-speed, low-drive capability signals.
- Reverse working voltage VRWM: This voltage should be higher than the normal operating voltage at the protected network terminal;
- IPP, Clamping Voltage, and Peak Pulse Power: These three parameters follow the P=UI relationship, the lower the clamping voltage, the safer the back-end device; ESD is easily weakened by factors such as structure, PCB capacitance, etc., so the discharged static electricity will not be fully applied to the network to be protected, making it difficult to estimate these parameters.
- Inter-layer capacitance CJ: Inter-layer capacitance that is too large will affect high-speed signal integrity;

We suggest:

(1) High-speed signal interface: CJ<1pF for USB2.0 interface

(2) Low-speed signal interface: (U)SIM interface CJ<10pF, UART interface, PCM interface CJ<20pF, TVS diodes or varistors can be used for ESD protection.

- Antenna Interface: If TVS components are used in the antenna interface, the RSE (Radiated Spurious Emission) may exceed the value defined in EN301489. Therefore, it is not recommended to use TVS on the antenna port. It is suggested to connect an inductor of 47nH~82nH for ESD protection.

6.5.2 ESD environmental control recommendations

(1) The processing equipment, testing instruments, tools, and equipment for electrostatic sensitive devices shall all be reliably grounded;

(2) The parts that come into contact with electrostatic sensitive components on equipment, instruments, tools, and fixtures, as well as moving parts near electrostatic sensitive components, are made of anti-static materials and have good grounding. The non-antistatic material parts undergo anti-static treatment.

(3) In the process of handling electrostatic sensitive devices such as ICs, single boards, modules, employees are correctly wearing static wrist straps or static gloves;

(4) Are there obvious anti-static labels and anti-static measures in the process of transporting and storing electrostatic sensitive devices?

Table 6-5 ESD performance parameters (Temperature: 25°C, Humidity: 40%)

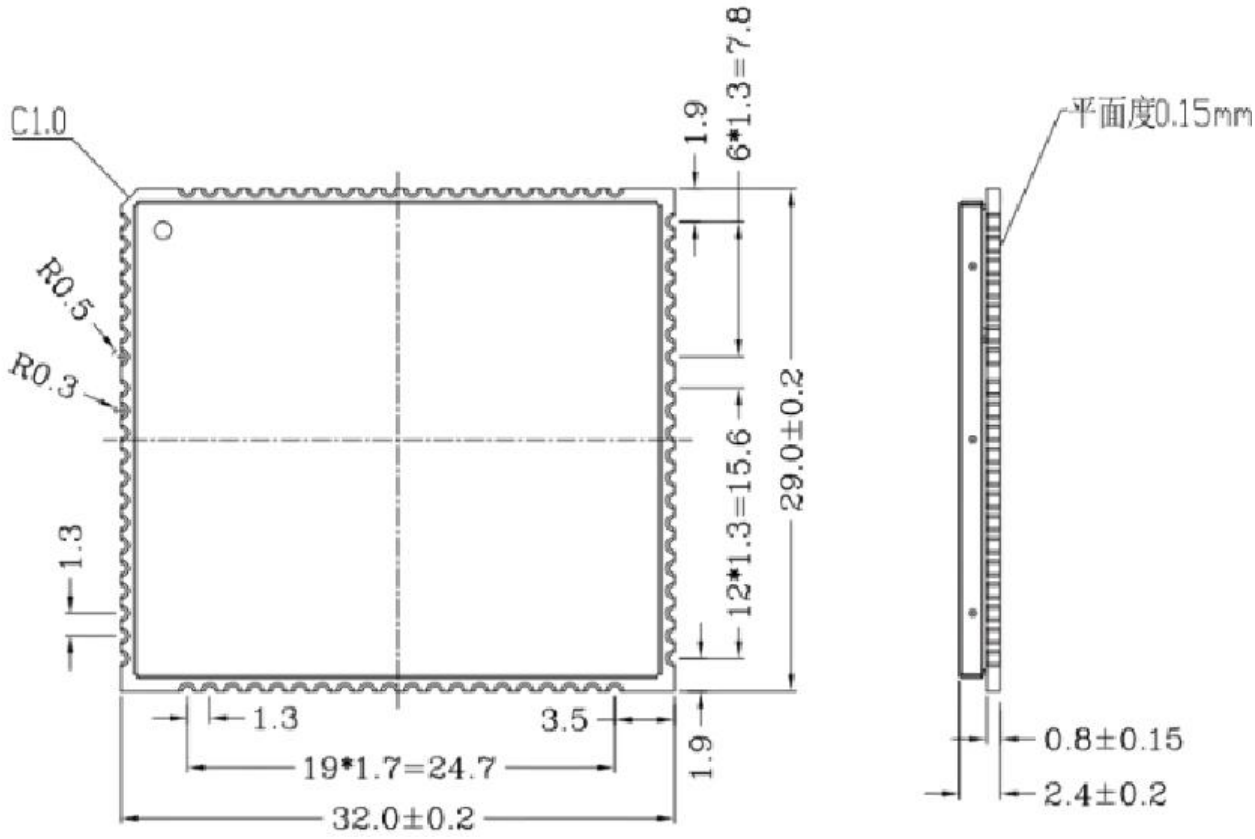
Pin name	Discharge phenomenon	Air discharge
VBAT,GND	+/-4kV	+/-8kV
Antenna interface	+/-4kV	+/-8kV
Others	+/-0.5kV	+/-2kV

Note

ESD results are all tested with development boards, the actual test results from customers' complete machines shall prevail.

7 Mechanical properties

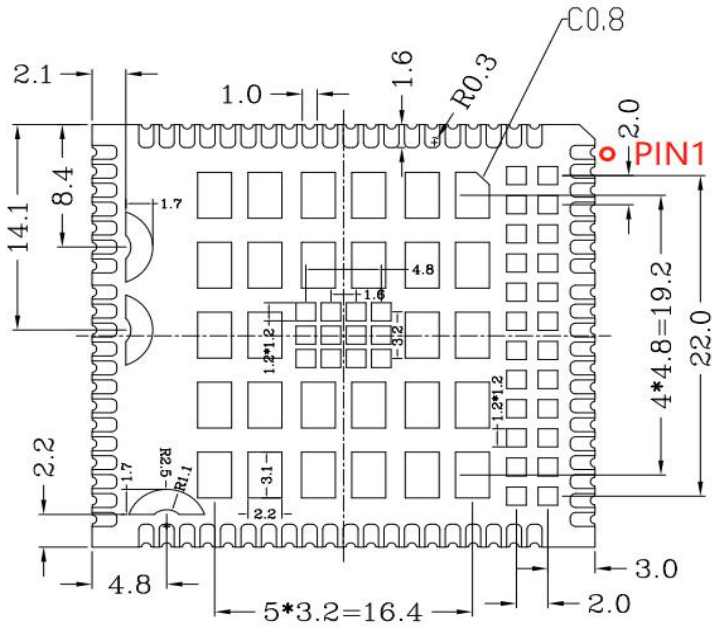
7.1 Mechanical dimensions



UNIT:mm

Figure 7.1 Module Mechanical Dimensional Drawing

7.2 Recommend encapsulation



UNIT:mm

Figure 7.2 Module Recommended Package (Bottom View)

Note

- To ensure the welding quality of the components and facilitate subsequent maintenance operations, the distance between the modules on the customer's motherboard and other components should be at least 3 mm.
- To ensure the reliability of soldering and pasting, it is recommended to maintain a minimum motherboard thickness of 1.2 mm.

7.3 Module rendering

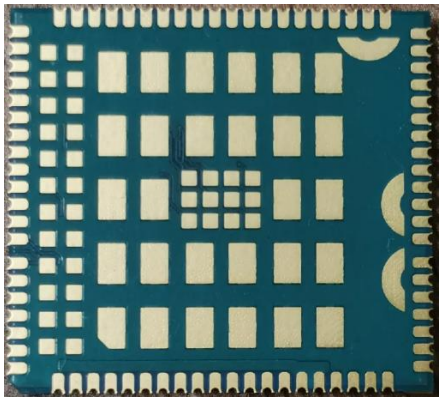
Top View  Bottom View

Figure 7.3 Module Top/Bottom View

The above is the design rendering of the module, please refer to the actual module for accuracy, especially the label content is for reference only.

7.4 Reflow curve

Here is the recommended reflow soldering profile chart provided by the module.

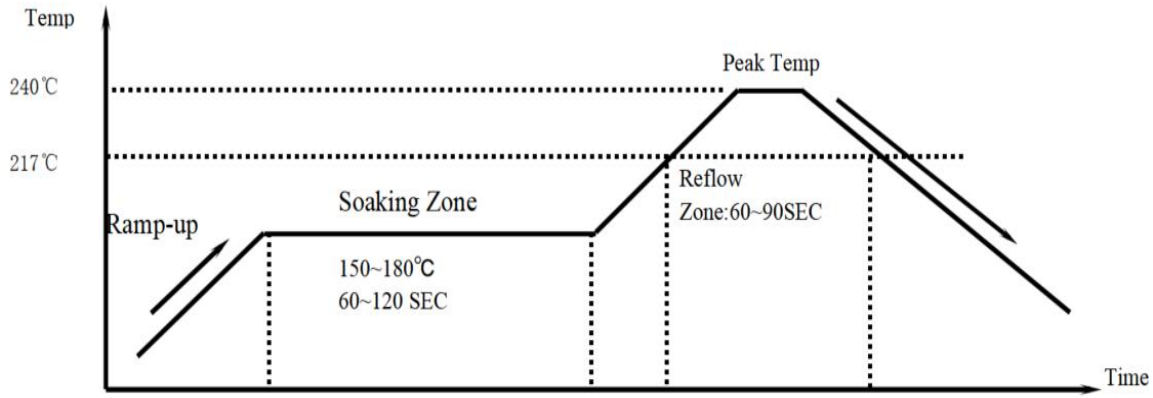


Figure 7.4 Soldering Reflow Curve for Module Recommendation

The following table shows the welding curve parameters.

Table 7-1 Welding Curve Parameters

	峰值温度	浸温	熔锡温度	上升斜率	降温斜率
Temp Range	240±5	150－180	217	25－150	
Time		60－120S	60－90S	0.5－4 ℃/s	≤4℃/s

7.5 PCB package design

Please contact our FAE to obtain the module PCB packaging file.

8 Production and packaging information

8.1 Storage conditions

The modules are shipped in the form of vacuum reel sealed bags, with a moisture sensitivity level of MSL 3.

Storage conditions:

- Temperature below 40°C, humidity below 90% (RH), can ensure 12 months of validity in well-sealed packaging.

Weldability.

- After unpacking, make sure 168 hours at a temperature below 30°C and relative humidity below 60% (RH)

Surface mount assembly is carried out inside.

If the above conditions are not met, baking is required:

- Roll wrapping, bake at 60°C±5°C for 24-48 hours
- If you need to accelerate the baking process, you should remove the module from the conveyor belt and place it on a heat-resistant container (such as a tray) for baking.

Bake (pay attention to ESD protection during the removal process) at 125°C ± 5°C for 8 hours.

- The cumulative baking time cannot exceed 96 hours.

Please refer to the IPC/JEDEC J-STD-033 standard for more detailed guidance.

8.2 Carrying adhesive wheel dimensions

The rubber wheel dimensions are as follows:

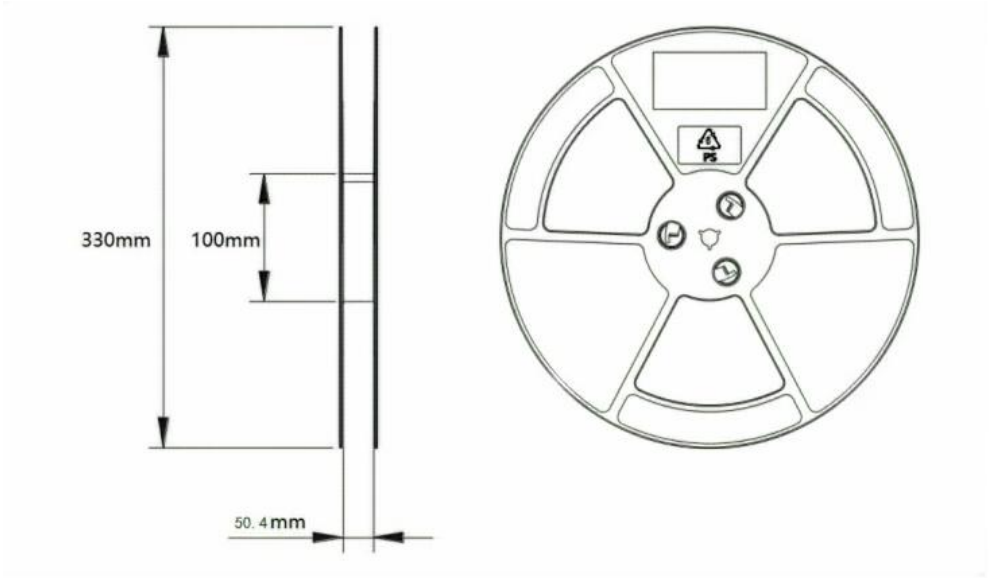
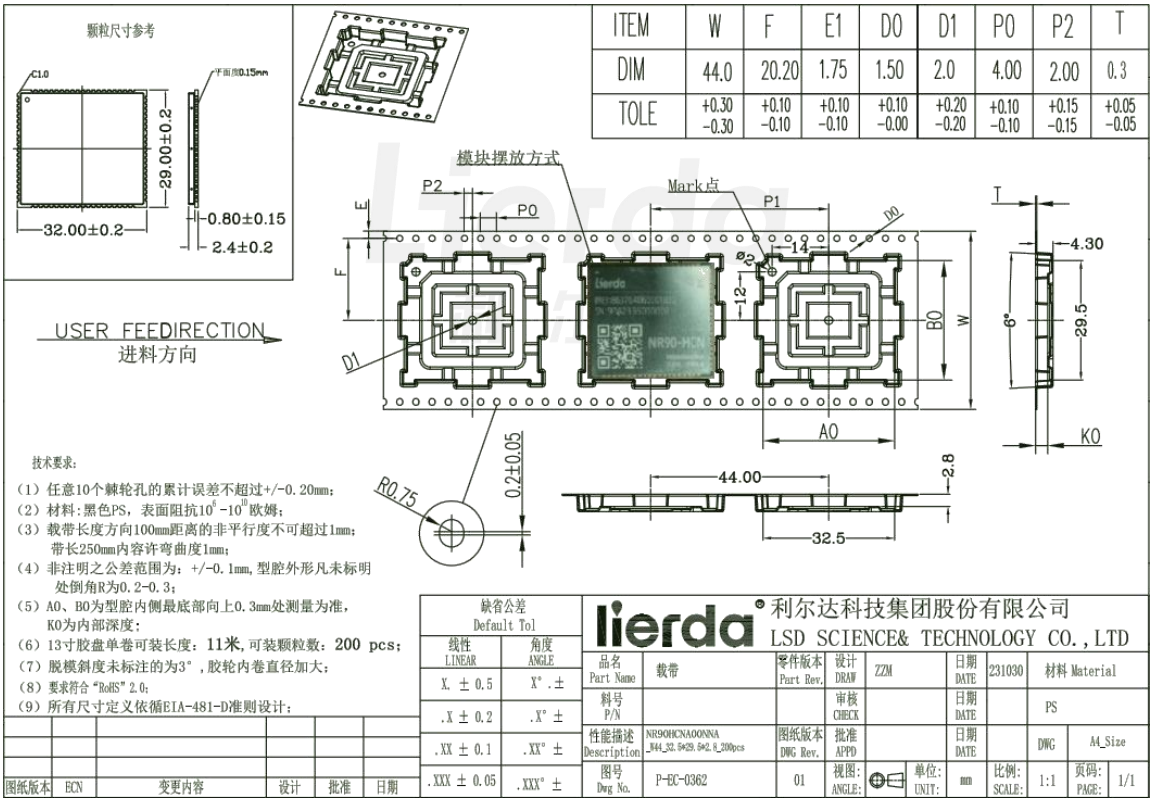


Figure 8.1 Rubber Wheel Dimension Diagram (unit:mm)

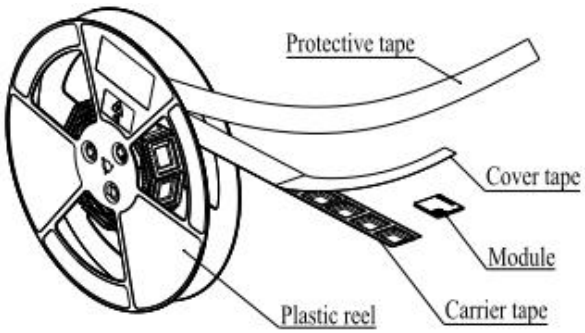
The dimensions of the conveyor belt are as follows:



ITEM	W	F	E1	D0	D1	P0	P2	T
DIM	44.0	20.20	1.75	1.50	2.0	4.00	2.00	0.3
TOLE	+0.30 −0.30	+0.10 −0.10	+0.10 −0.10	+0.10 −0.00	+0.20 −0.20	+0.10 −0.10	+0.15 −0.15	+0.05 −0.05

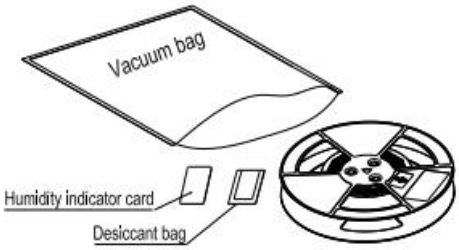
Figure 8.2 Conveyor Belt Dimension Diagram (unit:mm)

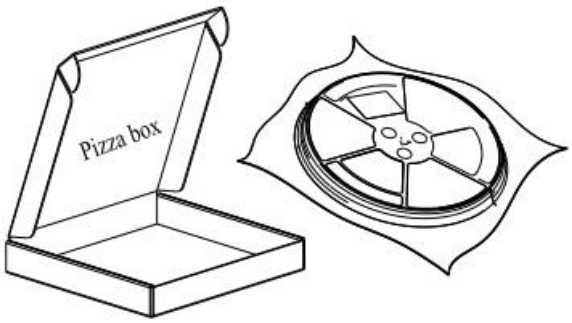
8.3 Packaging process



将模块放入载带中，使用上带热封；再将热封后的载带缠绕到胶盘中，用保护带缠绕防护。1个胶盘可装载 200 片模块。

将包装完成的胶盘、湿敏卡和干燥剂放入真空袋中，抽真空。





将抽真空后的胶盘放入披萨盒内。

将 5 个披萨盒放入 1 个卡通箱内，封箱。1 个卡通箱可包装1000片模块。

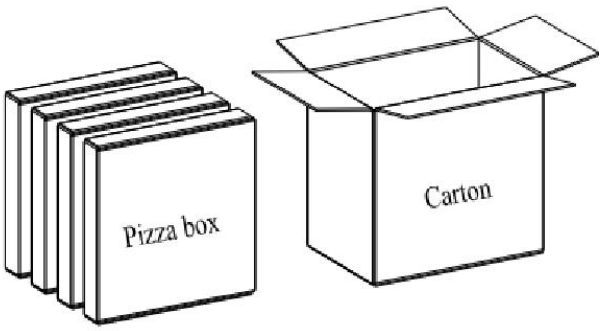


Figure 8.3 Packaging Process

9 Relevant documents and terminology abbreviations

Table 9-1 Related Documents

Serial number	Document Name	Annotation
[1]	NR90-HEA AT Command Manual	AT command set

Table 9-2 Term Abbreviations

Abbreviation	Full English name	Full name in Chinese
bps	bits per second	Per second
CPE	Customer-Premise Equipment	User ground equipment
FOTA	Firmware Over-The-Air	Firmware over-the-air differential upgrade
ESD	Electrostatic Discharge	Electrostatic discharge
FDD	Frequency Division Duplexing	Frequency Division Multiplexing
HSPA	High Speed Packet Access	High-speed data packet access
HSUPA	High Speed Uplink Packet Access	High-speed uplink data packet access
kbps	Kilo Bits Per Second	Thousand bits per second
LED	Light Emitting Diode	Light Emitting Diode
LTE	Long Term Evolution	Long-term evolution
Mbps	Mega Bits Per Second	Megabits per second
MIMO	Multiple-Input Multiple-Output	Multiple inputs, multiple outputs

Abbreviation	Full English name	Full name in Chinese
NR	New Radio	New Air Interface
PCIe	Peripheral Component Interconnect Express	Peripheral component interconnect standard
PCM	Pulse Code Modulation	Pulse Code Modulation
PPP	Point-to-Point Protocol	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation	Orthogonal Amplitude Modulation
QPSK	Quadrature Phase Shift Keying	Quadrature Phase Shift Keying
RC	Root Complex	Root complex
RF	Radio Frequency	Radio Frequency
RFFE	RF Front-End	RF front end
Rx	Receive	Receive
SCS	Subcarrier Spacing	Carrier spacing
SIMO	Single Input Multiple Output	Single Input Multiple Output
SMS	Short Message Service	Short Message Service
Tx	Transmit	Send
UART	Universal Asynchronous Receiver & Transmitter	Universal asynchronous receiver-transmitter
USB	Universal Serial Bus	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module	(Global) User Identification Module
VIH	Input High Voltage Level	Enter high voltage level
VIL	Input Low Voltage Level	Enter low voltage level
VOH	Output High Voltage Level	Output high voltage level
VOL	Output Low Voltage Level	Output low voltage level

Abbreviation	Full English name	Full name in Chinese
WCDMA	Wideband Code Division Multiple Access	Broadband code division multiple access
RedCap	Reduced Capability	Reduce capability