Lierda NT26-FEU D Series Hardware design manual

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Revision history of the document

Document version	Change date	Reviser	Reviewer	Change content
Rev1.0	25-02-08	CWY、SZ	SLY、YMX	First edition

Safety instructions

Users are responsible for complying with the relevant regulations of other countries regarding wireless communication modules and devices, as well as specific environmental regulations for use. By following the following safety principles, personal safety can be ensured and help protect products and work environments from potential damage. Our company is not responsible for any losses related to customers' failure to comply with these regulations.

	Road safety comes first! Do not use handheld mobile devices while driving unless they have hands-free functionality. Please park your car before making a phone call!
	Please turn off your mobile terminal device before boarding. The wireless function of the mobile terminal is prohibited from being turned on in the airplane to prevent interference with the aircraft communication system. Ignoring this prompt may compromise flight safety or even violate the law.
	When in a hospital or health care facility, pay attention to any restrictions on the use of mobile terminal devices. RF interference can cause medical equipment to malfunction, so it may be necessary to turn off mobile terminal devices.
	Mobile terminal devices do not guarantee effective connection in any situation, such as when there is no credit on the mobile terminal device or the SIM card is invalid. When you encounter the above situation in an emergency, remember to use emergency calls, and make sure your device is powered on and in an area with sufficient signal strength.
	Your mobile terminal device will receive and emit radio frequency signals when it is turned on. When it is close to a TV, radio, computer, or other electronic devices, it will generate radio frequency interference.
	Please keep the mobile terminal device away from flammable gas. When you are near gas stations, oil depots, chemical plants, or explosive operation sites, please turn off the mobile terminal device. Operating electronic devices in any potentially explosive hazardous location poses a safety risk.

Module selection for application

Serial number	Module model	Support frequency band	Dimensions (mm)	Module introduction
1	NT26FEUD60NNA	Band1/3/5/7/8/20/28 /38/40/41	17.7×15.8×2.4	European version

Content

1 Introduction

This document defines the application specifications of the Lierda NT26-FEU D series Cat.1 wireless communication module, describing its frequency band functions, key features, hardware interfaces, operating modes, electrical characteristics, mechanical specifications, packaging storage, etc. It can help users quickly grasp the application methods of this Cat.1 module and quickly and flexibly carry out product design.

For the sake of convenience in narration, the NT26-FEU D series Cat.1 wireless communication module mentioned later in this document will be uniformly referred to as the "NT26-FEU D module".

2 Product Overview

NT26-FEU D module is a leading Cat.1 wireless communication module globally, compliant with 3GPP R14 Cat.1bis standard, supporting bandwidths of 1.4/3/5/10/15/20MHz, with features such as small size, low power consumption, and strong anti-interference capability. NT26-FEU D module is suitable for various common IoT application scenarios, such as:

- Smart meter reading
- Smart Parking
- Smart City
- Intelligent security
- Asset Tracking
- Smart home appliances
- Agriculture and environmental monitoring

2.1 Frequency band and function

The wireless network functions supported by the module are as follows:

Table 2-1 Module Supports Wireless Network Function

Network function	Explanation
LTE	LTE-FDD/LTE-TDD
WIFI	WIFI Scan

The supported wireless communication protocols of the module are as follows:

Table 2-2 Module Supports Wireless Network Standards

Wireless network standard	Band
LTE-FDD	B1/B3/B5/B7/B8/B20/B28
LTE-TDD	B38/B40/B41(140 MHz)

2.2 Key Features

Key features of the module are as follows:

Table 2-3 Module Key Characteristics Description

Parameters	Explanation
Module packaging	LCC+LGA
Module size	17.7mm×15.8mm×2.4mm (L×W×H)
Module weight	1.5g
Operating voltage	VBAT power supply range: 3.3～4.5V, typical value: 3.8V
VDD_EXT characteristics	The D series provides two hardware versions. Sleep mode: VDD_EXT power off (default) Sleep mode: VDD_EXT not power off (reserved)
Ultra low power	Sleep mode: 3uA (typical value)
Transmit power	23dBm±2.7dB（Max）
Antenna Interface	50Ω characteristic impedance
USIM	Supported USIM card types: Class B (3.0 V) and Class C (1.8 V)
UART	Main serial port: ◆ Used for AT command transmission and data transfer, the supported baud rate defaults to 115200bps. ◆ Used for firmware upgrade, the supported default baud rate is 921600bps
	Debug serial port: ◆ Used for software debugging. ◆ The default baud rate of the serial port is 3Mbps
	Auxiliary serial port: ◆ User-defined function
USB	◆ Compatible with USB 2.0 (supporting host mode only), with a maximum data transfer rate of 480 Mbps ◆ Used for AT command transmission, data transfer, software debugging, and firmware upgrades
I2C	Support I2C function

SPI	Support SPI function
PCM	Support PCM function
SPK	Support SPK function
CAMERA	Software adaptation can support camera functionality.
LCD	Software adaptation can support LCD functions.
Indicator light	◆ Operating status indicator ◆ Network status indicator
Communication interface characteristics	Support 3GPP Rel.13/14 Cat.1 wireless communication interface and protocol.
Network protocol features	Support protocols such as TCP/UDP/HTTP(S)/SSL/MQTT(S)/FOTA/PPP/RNDIS/FTP/ECM
Data transmission characteristics	◆ LTE-FDD: Maximum downlink speed of 10Mbps, maximum uplink speed of 5Mbps ◆ LTE-TDD: Maximum downlink speed 8.96Mbps, maximum uplink speed 3.1Mbps
Firmware upgrade	◆ Main Serial Port Upgrade ◆ USB interface upgrade ◆ DFOTA Upgrade
Operating temperature	◆ Normal operating temperature range(1): -35~75℃ ◆ Extended operating temperature range(2): -40~85℃
Storage temperature	Storage temperature range(3): -40~90℃
RoHS	All components comply with RoHS standards.

Note 1, 2, 3: See section 6.6 for specific descriptions regarding temperature.

2.3 Function block diagram

NT26-FEU D series module has rich peripheral interfaces and RF functions, the functional block diagram is as follows:

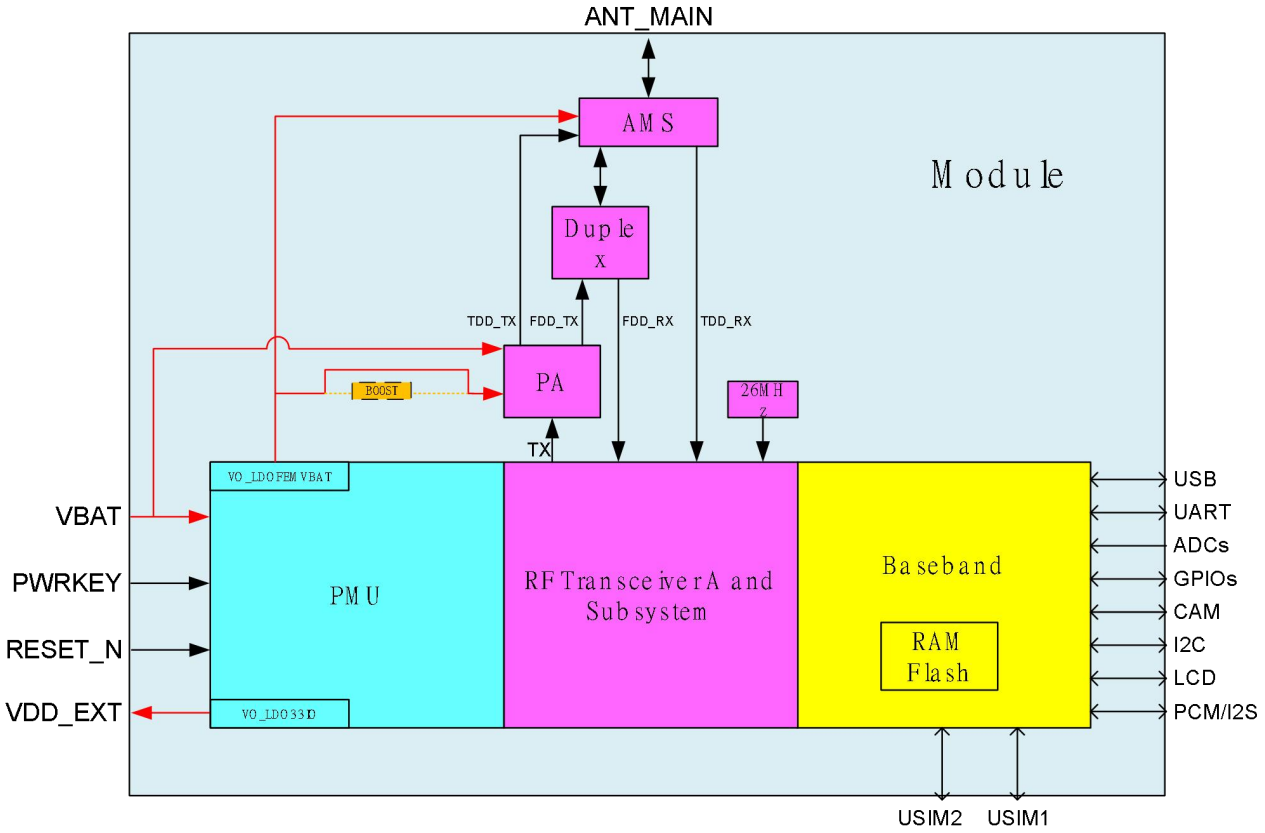


Figure 2.1 Module Functional Block Diagram

2.4 Pinout diagram

NT26-FEU D series module has a total of 109 pins, with 48 LCC pins and the remaining 61 LGA pins. The pin distribution diagram of the module is as follows:

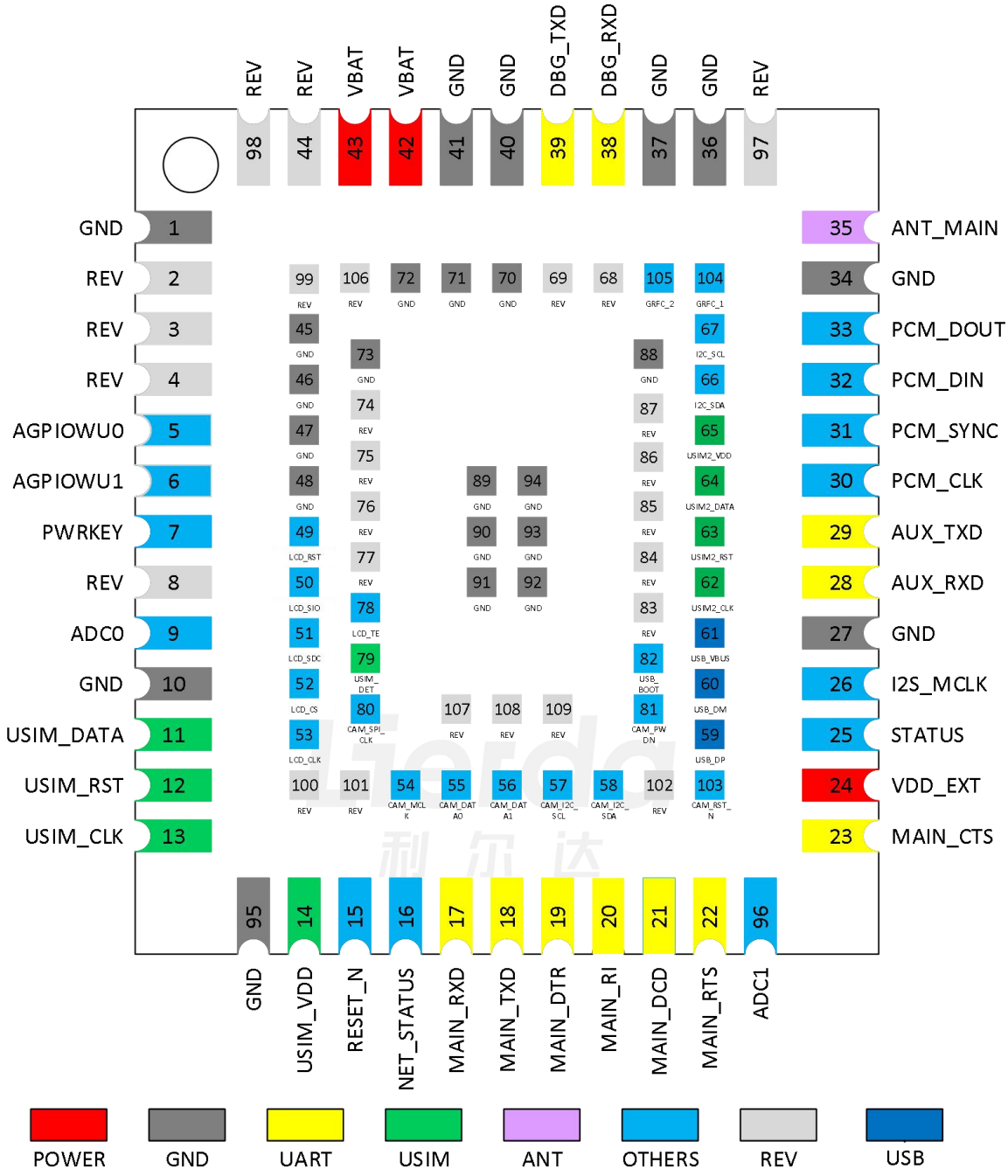


Figure 2.2 Module Pinout Diagram

2.5 Pin Description Table

In order to better understand the application, the following table is an explanation of the type definition of I/O parameters:

Table 2-4 Explanation of I/O Parameter Type Definitions

I/O parameter type	Explanation
DI	Numeric input
DO	Numeric output
DIO	Numeric input and output
AI	Simulated input
AO	Simulated output
AIO	Simulated input and output
PI	Power input
PO	Power output
G	Grounding
OD	Leakage path opening

In order to better understand the application, the following table describes the characteristics of the power domain parameters:

Table 2-5 Module Power Domain Characteristics Explanation

Power domain parameters Type	DC characteristics	Explanation	Power supply object
VBAT	Vmax=4.5V Vmin=3.3V Vnorm=3.8V	Module power input, recommended to use 3.8V/1.2A power supply	Module
VDD_EXT	VILmax=0.2×VDD_EXT VIHmin=0.7×VDD_EXT VOLmax=0.15×VDD_EXT VOHmin=0.8×VDD_EXT	Default 1.8V; Different hardware versions: In sleep mode, VDD_EXT power-off version, driving capability is 120mA; In sleep mode, VDD_EXT non-power-down version, driving capability is 3mA.	VDD_EXT

VO_LDOIO	VOLmax=0.2×VO_LDOIO VOHmin=0.7×VO_LDOIO VILmax=0.15×VO_LDOIO VIHmin=0.8×VO_LDOIO	Default 1.8V, configurable by software; Power off in sleep mode	UART GPIO
VDD18AON	VILmax=0.2×VDD18AON VIHmin =0.7×VDD18AON VOLmax=0.15×VDD18AON VOHmin=0.8×VDD18AON	No power consumption in sleep mode	WAKEUP RESET
LDO_AONIO	VILmax=0.2×LDO_AONIO VIHmin =0.7×LDO_AONIO VOLmax=0.15×LDO_AONIO VOHmin=0.8×LDO_AONIO	Default 1.8V, configurable by software; No power consumption in sleep mode.	AGPIO
VO_LDOSIM	Vnorm=1.8/3.0V VOLmax=0.15×VO_LDOSIM VOHmin=0.8×VO_LDOSIM VILmax=0.2×VO_LDOSIM VIHmin=0.7×VO_LDOSIM	SIM card dedicated power supply, supporting cards of 1.8/3.0V	USIM

Table 2-6 Module Pin Description

1. Power - POWER					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**
42,43	VBAT	PI	Power supply	Vmax=4.5V Vmin=3.3V Vnorm=3.8V	The external power supply needs to provide a current carrying capacity of 1.2A or above.
24	VDD_EXT	PO	Power output	Vnorm=1.8V $I_O$max=120mA	Can be used for external circuit pull-up or reference level; defaults to power off in sleep mode; leave floating if not used, it is recommended to reserve test points.
1,10,27,34,36, 37,40,41,45~48,	GND	G	Grounding	-	

70~73,88~95					

2. Power on/off and reset					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**
7	PWRKEY	DI	Module power on/off pin	V_{IL}max=0.45V	Internal pull-up, low level effective, if not used, leave floating.
15	RESET_N	DI	Module reset pin	V_{IL}max=0.45V	Internal pull-up, active low, leave floating if not used.

3、USB					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**
59	USB_DP	DIO	USB differential data (+)	-	If not used, leave floating
60	USB_DM	DIO	USB differential data (-)	-	
61	USB_VBUS	DI	USB_VBUS input wake-up	-	

4. Serial port UART					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**
17	MAIN_RXD	DI	Main serial port	VO_LDOIO	

			receives data		
18	MAIN_TXD	DO	Main serial port sends data	VO_LDOIO	
19	MAIN_DTR	DI	Main serial port data terminal ready	LDO_AONIO/ VDD18AON	AGPIO function, power domain LDO_AONIO, no power loss during sleep. WAKEUP function, power domain VDD18AON, no power loss during sleep
20	MAIN_RI	DO	Main serial port outputs ringing prompt.	LDO_AONIO	
21	MAIN_DCD	DO	Main serial port output carrier detection	VO_LDOIO	
22	MAIN_RTS	DO	Main serial port DTE clear to send	VO_LDOIO	
23	MAIN_CTS	DI	Main serial port DTE requests to send	VO_LDOIO	
38	DBG_RXD	DI	Debugging serial port receiving data	VO_LDOIO	
39	DBG_TXD	DO	Debugging serial port to send data	VO_LDOIO	
28	AUX_RXD	DI	Assist serial port to receive data	VO_LDOIO	Not supported temporarily.
29	AUX_TXD	DO	Assist in sending data through the serial port	VO_LDOIO	Not supported temporarily

5. USIM card interface					
Pin	**Pin name**	**I/O**	**Description**	**DC**	**Note**

numbe r				characteristi cs	
11	USIM_DATA	DIO	SIM card data cable	VO_LDOSIM	
12	USIM_RST	DIO	SIM card reset line	VO_LDOSIM	
13	USIM_CLK	DIO	SIM card clock line	VO_LDOSIM	
14	USIM_VDD	PO	SIM card power	VO_LDOSIM	1.8/3.0V
79	USIM_DET	DI	Detection of SIM card status signal	VDD18AON	High-level effective
62	USIM2_CLK	DIO	SIM card 2 clock line	VO_LDOIO	USIM2 pin is multiplexed with the CAMERA section pins.
63	USIM2_RST	DIO	SIM card 2 reset line	VO_LDOIO	
64	USIM2_DATA	DIO	SIM card 2 data cable	VO_LDOIO	
65	USIM2_VDD	PO	SIM card 2 power	1.8/3.0V $I_O$max=50mA	Same power supply as USIM_VDD

6. Antenna RF interface					
Pin numbe r	Pin name	I/O	Description	DC characteristics	Note
35	ANT_MAIN	AIO	RF antenna interface	50Ω characteristic impedance	
104	GRFC_1*	DIO	RF control signal	1.8V	If not used, leave floating
105	GRFC_2*	DIO	RF control signal	1.8V	If not used, leave floating

7. Camera interface					
Pin numb	Pin name	I/O	Description	DC Characteristic	Note

er				s	
54	CAM_MCLK	DO	Camera main clock	VO_LDOIO	If not used, leave floating
55	CAM_DATA0	DIO	Camera data D0	VO_LDOIO	If not used, leave floating
56	CAM_DATA1	DIO	Camera data D1	VO_LDOIO	If not used, leave floating
57	CAM_I2C_SCL	OD	Camera I2C clock	VO_LDOIO	Recommend external pull-up, leave floating if not used.
58	CAM_I2C_SDA	OD	Camera I2C data	VO_LDOIO	Recommend external pull-up, leave floating if not used.
80	CAM_SPI_CLK	DO	Camera SPI clock	VO_LDOIO	If not used, leave floating
81	CAM_PWDN	DO	Camera off	VO_LDOIO	If not used, leave floating
103	CAM_RST_N	DO	Camera reset	VO_LDOIO	If not used, leave floating

8. LCD interface					
Pin number	Pin name	I/O	Description	DC characteristics	Note
49	LCD_RST	DO	LCD reset	VO_LDOIO	If not used, leave floating

50	LCD_SIO	DIO	LCD data output	VO_LDOIO	If not used, leave floating
51	LCD_SDC	DO	LCD data address switching signal	VO_LDOIO	If not used, leave floating
52	LCD_CS	DO	LCD chip select	VO_LDOIO	If not used, leave floating
53	LCD_CLK	DO	LCD clock	VO_LDOIO	If not used, leave floating
78	LCD_TE	DI	LCD frame synchronization	LDO_AONIO	If not used, leave floating

9. I2C Interface					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**
66	I2C_SDA	DIO	I2C serial data	VO_LDOIO	If not used, leave floating
67	I2C_SCL	DO	I2C serial clock	VO_LDOIO	If not used, leave floating

10, PCM interface					
Pin number	**Pin name**	**I/O**	**Description**	**DC Characteristics**	**Note**
30	PCM_CLK	DO	PCM clock output	VO_LDOIO	If not used, leave floating
31	PCM_SYNC	DO	PCM synchronization signal	VO_LDOIO	If not used, leave floating
32	PCM_DIN	DI	PCM data input	VO_LDOIO	If not used, leave floating

33	PCM_DOUT	DO	PCM data output	VO_LDOIO	If not used, leave floating
26	PCM_MCLK	DO	PCM reference clock	VO_LDOIO	If not used, leave floating

11. SPK Interface					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**
5	AGPIOWU0	DIO	AGPIO function, power domain LDO_AONIO, no power loss during sleep. WAKEUP function, power domain VDD18AON, no power loss during sleep	LDO_AONIO/ VDD18AON	If not used, leave floating
6	AGPIOWU1	DIO	AGPIO function, power domain LDO_AONIO, no power loss during sleep. WAKEUP function, power domain VDD18AON, no power loss during sleep	LDO_AONIO/ VDD18AON	If not used, leave floating

12, ADC interface					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**

9	ADC0	AI	ADC0 interface	Internal direct connection Input voltage range: 0~1.6V	If not used, leave floating
96	ADC1	AI	ADC1 Interface	Internal partial pressure Input voltage range: 0~3.3V Default 1.6V Internal partial pressure can be enabled through the software.	If not used, leave floating

13. Status indication					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**
16	NET_STATUS	DO	Network status indication	LDO_AONIO	If not used, leave floating
25	STATUS	DO	Operating status indication	LDO_AONIO	If not used, leave floating

14. Other interfaces					
Pin number	**Pin name**	**I/O**	**Description**	**DC Characteristics**	**Note**
82	USB_BOOT	DI	Emergency download mode control. Pull up to VDD_EXT before the module is powered on, and the module will enter emergency download mode after startup.	VO_LDOIO	The module defaults to weak pull-down internally, it is recommended to leave it floating.

15, keep the interface					
Pin number	**Pin name**	**I/O**	**Description**	**DC characteristics**	**Note**
2~4,8,44,68,69,74~77,83~87,97~99,100~102,106~109	REV	-	-	-	Undefined pins, suggest leaving floating, where pin 8 inside the module can be configured as CAM_VDD by selecting the corresponding pad.

Note: "*" indicates that the feature is under development.

2.6 Evaluation suite

Lierda can provide a complete evaluation and development kit, including module adapter boards, Cat.1 & NB-IoT module universal development boards, etc. Please feel free to contact for consultation.

3 Work characteristics

3.1 Working mode

NT26-FEU D series modules have multiple operating modes. The following table briefly describes several common operating modes of the modules:

Table 3-1 Working Modes

Pattern	Status description
Normal working mode	Data transmission: Network connection is normal. Module power consumption depends on network settings and data transmission rate.
	Idle state: Software running normally. The module is connected to the network but not exchanging data with it.
Minimum functionality mode	AT+CFUN=0 can set the module to minimum functionality mode, where both RF and USIM card are not working.
Sleep mode	The module's power consumption will be reduced to a minimum, but the module can still receive paging, short messages, and TCP/UDP data.
Shutdown mode	VBAT power supply is not disconnected, software stops working.

Note: Please refer to the AT command data manual for related AT+CFUN instructions.

3.2 Sleep mode

The module can enter sleep mode via AT commands. In sleep mode, the module can reduce power consumption to a very low level while still being able to receive network information through RF.

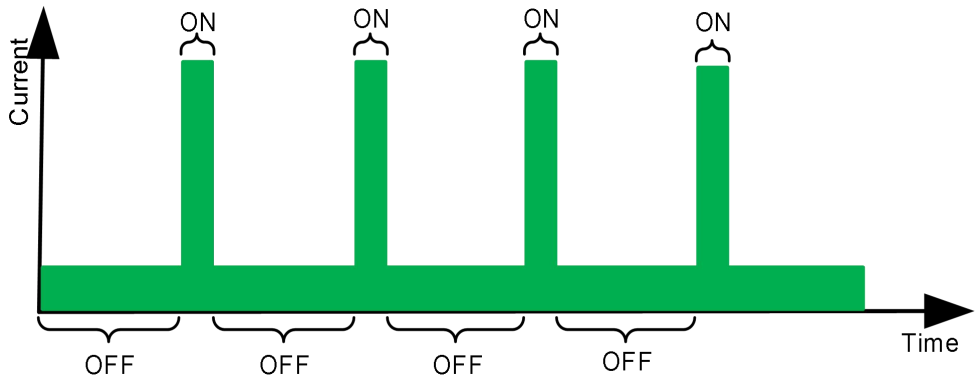


Figure 3.1 Power Consumption State of the Module in Sleep Mode

In sleep mode, the module peripherals are powered off to reduce power consumption, but the RF is in intermittent reception state and can still receive network information. When the module has URC to report, it will wake up the host through the MAIN_RI pin.

3.2.1 Main serial port application scenarios

If the module and the host communicate via UART, the module needs to meet the following 2 conditions to enter sleep mode:

◆ Enable sleep mode by executing the command AT+QSCLK=1;

◆ Ensure that MAIN_DTR remains at a high level or floating.

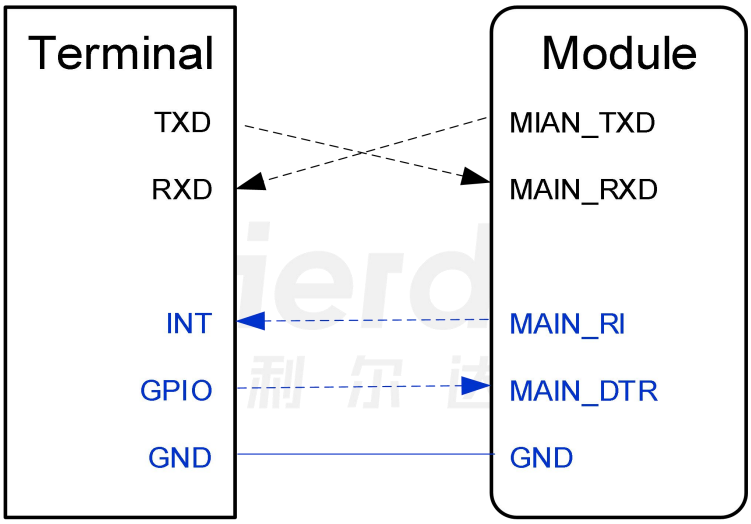


Figure 3.2 Application Circuit of Sleep Mode UART

◆ When the module needs to report URC, the module notifies the host through MAIN_RI.

◆ The host can wake up the module by pulling down MAIN_DTR.

◆ If the host continues to pull down MAIN_DTR, it can prevent the module from entering sleep mode.

◆ If you enable the sleep function with AT+QSCLK=2, you can wake up the module by sending any command to the main UART interface.

3.2.2 USB application scenarios

In the USB application scenario, the module needs to meet the following 3 conditions at the same time to enter sleep mode:

◆ Perform AT+QSCLK=1;

◆ Ensure MAIN_DTR remains at a high level or floating;

◆ The host USB bus connected to the module's USB interface enters a suspended state.

3.2.2.1 Support USB remote wake-up function

The host supports USB suspend and resume, as well as USB remote wake-up functions.

Please refer to the diagram for the connection between the module and the host:

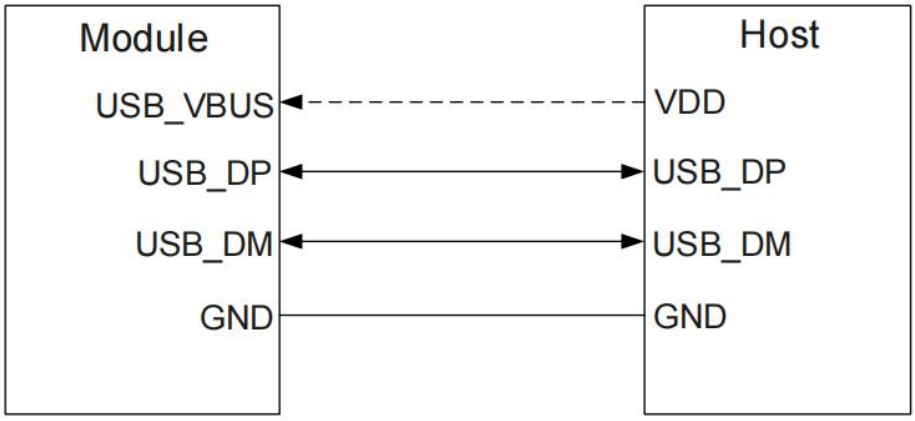


Figure 3.3 Sleep application with USB remote wake-up function

◆ Sending data to the module via USB will wake up the module.

◆ When the module reports URC, the module will send a remote wake-up signal via the USB bus to wake up the host.

3.2.2.2 Support USB suspend and wake up and MAIN_RI function.

If the host supports USB suspend and resume but does not support USB remote

wake-up function, the host needs to be woken up by the MAIN_RI signal of the module.

Connection between the module and the host reference the following diagram:

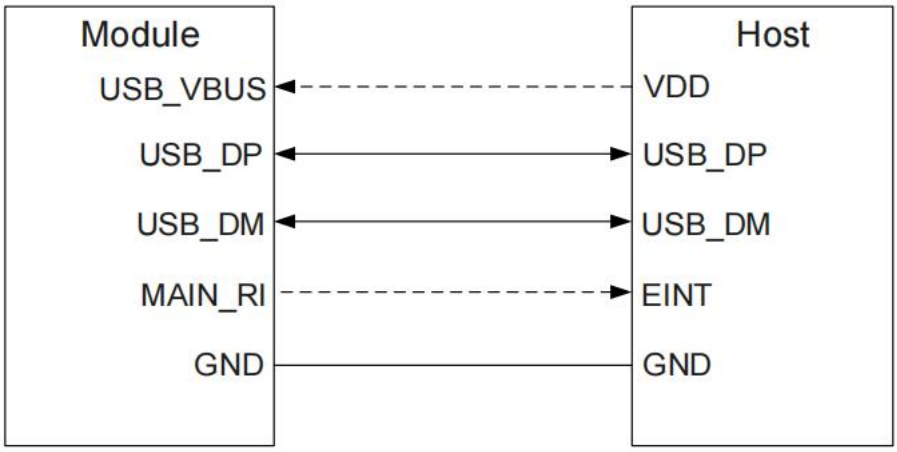


Figure 3.4 Sleep Application with MAIN_RI Function

- Sending data to the module via USB will wake up the module;
- When the module reports URC, the module can wake up the host through MAIN_RI.

3.2.2.3 Does not support USB suspend function.

When the host does not support USB suspend function, the module needs to meet the following 3 conditions to enter sleep mode:

- Execute AT+QSCLK=1;
- Ensure that MAIN_DTR remains at a high level or floating;
- Disconnect USB_VBUS power supply.

If the host does not support USB suspend function, the module can enter sleep mode by disconnecting USB_VBUS through an external control circuit.

Connection between module and host reference the following diagram:

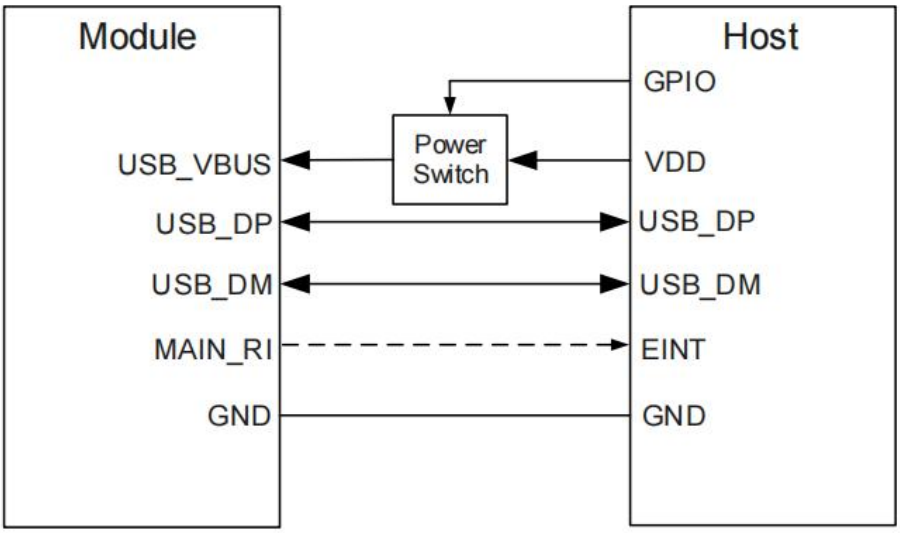


Figure 3.5 Sleep application that does not support USB suspend functionality

Note: Restore USB_VBUS power supply to wake up the module.

3.3 Airplane mode

When the module enters flight mode, the RF function cannot be used, and all AT commands related to RF cannot be accessed. The module can enter flight mode in the following ways:

You can set it by sending the AT+CFUN=<fun> command. The <fun> parameter can be set to 0 or 1.

◆ AT+CFUN=0: Minimum functionality mode (turn off RF function and USIM card).

◆ AT+CFUN=1: Full functionality mode (default).

3.4 Power supply design

3.4.1 Power supply introduction

NT26-FEU D module provides 2 VBAT pins for connecting to an external power source, and VDD_EXT is the power output of the module for external reference voltage. The interface description is as follows:

Table 3-2 Power Supply Pin Definitions

Pin number	Pin name	Description	Minimum value	Typical value	Maximum value	Unit
42,43	VBAT	Module power supply	3.3	3.8	4.5	V
24	VDD_EXT	Power output	-	1.8	-	V

The VBAT power supply range of the module is 3.3 to 4.5V, and it is necessary to ensure that the minimum input voltage when the module is working does not drop below 3.3V. The following figure illustrates the VBAT voltage drop situation of the module during burst transmission:

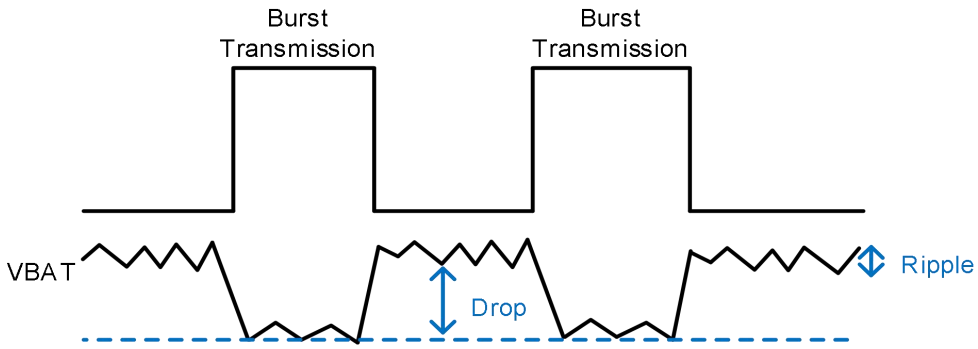


Figure 3.6 Requirements for emergency transmission power supply

The VDD_EXT of the module can provide pull-up for external GPIO. In sleep mode, VDD_EXT defaults to power off.

3.4.2 Power supply design

When the module is operating at the maximum transmission power in a 4G network, the transient operating current under the current network can reach 1.2A, which may cause a drop in the power supply voltage. In any case, it is necessary to ensure that the module power supply voltage remains above 3.3V, otherwise the module may experience unexpected conditions such as rebooting. To reduce voltage drops, it is recommended to use a low ESR (ESR <0.7Ω) 100uF filtering capacitor. It is also recommended to reserve three chip multilayer ceramic capacitors (MLCC) with good ESR performance for VBAT, and the capacitors should be placed close to the VBAT pin. Additionally, it is recommended to add a high-power, low-clamping voltage TVS diode with a high reverse pulse current Ipp at the VBAT terminal to improve the module's surge voltage withstand capability.

Power reference circuit as follows:

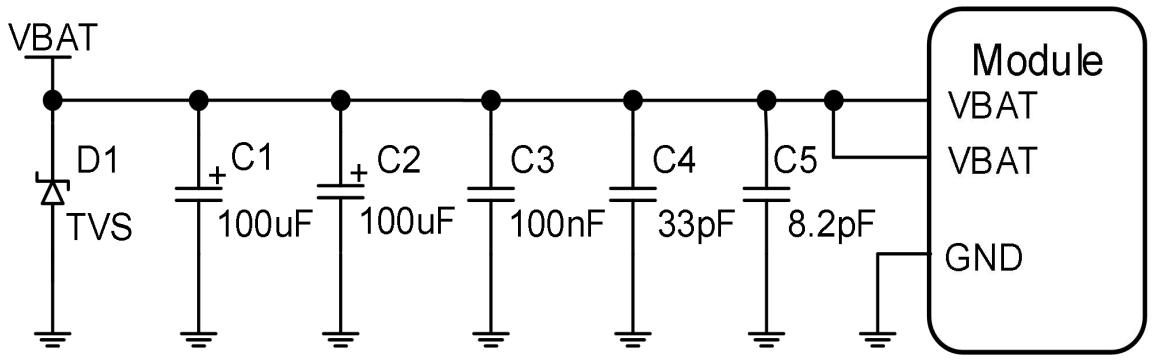


Figure 3.7 Module Power Supply Circuit Reference

In PCB design, the longer the VBAT trace, the wider the trace width should be. It is recommended that the trace width should not be less than 2mm. The GND plane in the power section should be as complete as possible with multiple ground vias. Also, place decoupling capacitors as close as possible to the VBAT pin of the module.

◆ D1 is a TVS tube with high power and low clamping voltage;

◆ C1, C2 are 100uF low ESR tantalum capacitors, which improve the power supply's ripple current capability and stabilize voltage.

◆ C3~C5 are ceramic packaged filtering capacitors of 100nF, 33pF, and 8.2pF respectively, used to eliminate high-frequency interference.

3.5 Power on and off

3.5.1 Introduction to power on and off

The module can be powered on and off through the PWRKEY pin. The pin description is as follows:

Table 3-3 PWRKEY Pin Description

Pin number	Pin name	I/O	Description	Note
7	PWRKEY	DI	Module power on and off, low	Default to high level

			level effective	

◆ The module can be powered on by pulling down PWRKEY for at least 500ms in the shutdown state;

◆ When the module is powered on, pull down the PWRKEY to a low level, hold it for at least 650ms, and then shut down.

In addition, you can also power off by using the AT command: AT+QPOWD.

Precautions

◆ When the module is working normally, do not immediately cut off the power supply to the module, as this may damage the Flash data inside the module. It is recommended to first power off the module using the PWRKEY or AT command before disconnecting the power supply.

◆ When shutting down using the AT command, please make sure that after the shutdown command is executed, the PWRKEY remains at a high level, otherwise there may be a situation of restarting after shutdown, and disconnecting the power at this time may damage the Flash.

◆ If the PWRKEY is often grounded to power on, it is recommended to use AT+QPOWD to execute the shutdown process before disconnecting the power.

3.5.2 Reference design for power on/off circuit

Recommended to use an open-drain drive circuit or directly control the power switch through a button. To prevent electrostatic discharge generated by contact, place a TVS near the button for ESD protection. Please refer to the circuit below:

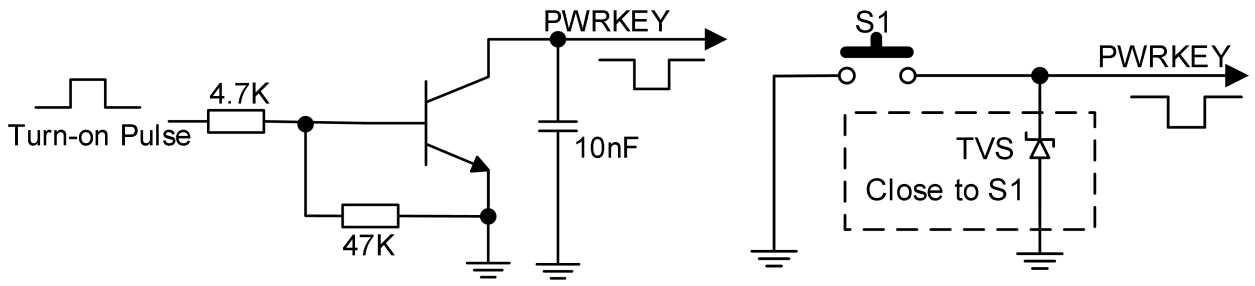
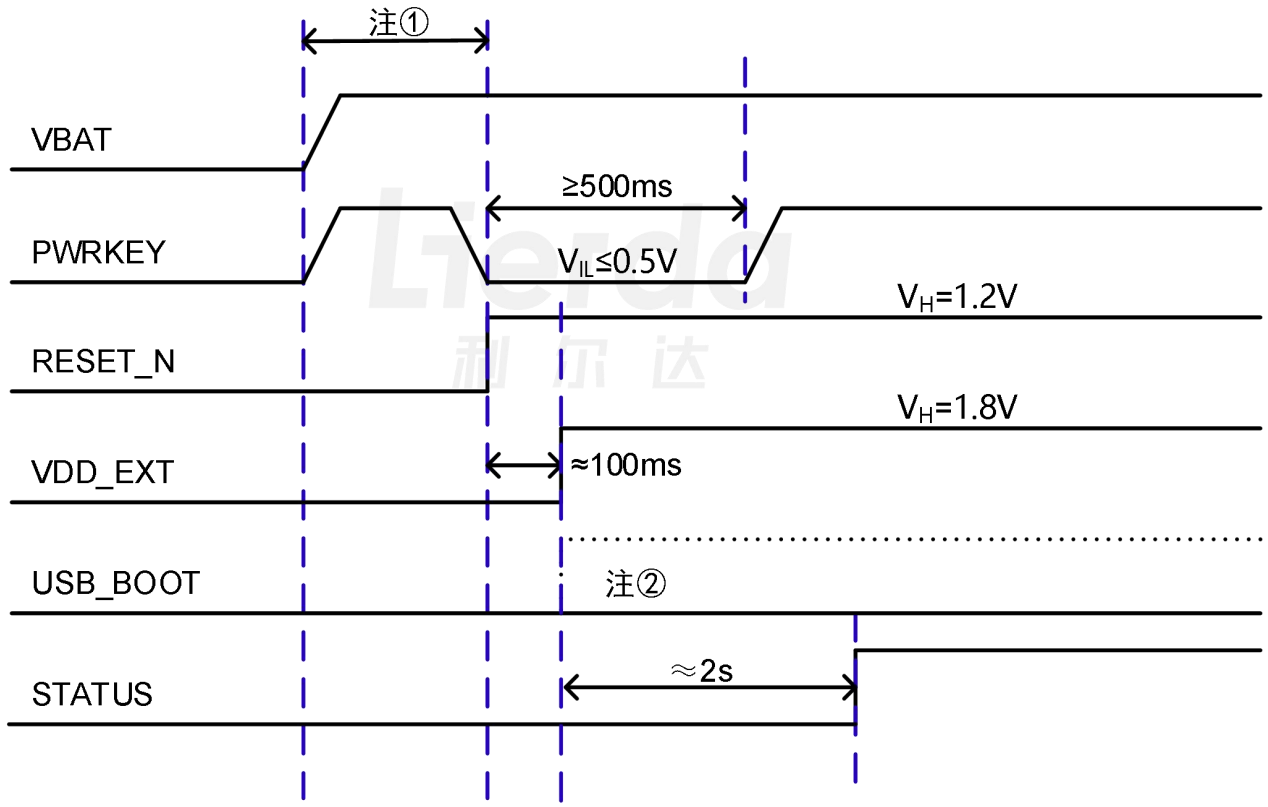


Figure 3.8 Power On/Off Circuit

3.5.3 Power-on sequence

The power-on sequence of the module is as shown in the following figure:



Notes:

Note 1: The initial state of VBAT when powered on needs to be less than 0.1V, and the time for VABT to rise from 0V to 2.5V should be less than 10ms; before pulling down the PWRKEY pin, ensure the stability of the VBAT voltage, it is recommended to pull down the

PWRKEY pin from the time VBAT is powered on.

The time interval between them should not be less than 30ms.

Note 2: Pull the USB_BOOT pin to VDD_EXT before powering on the module, and the module will enter emergency download mode when powered on.

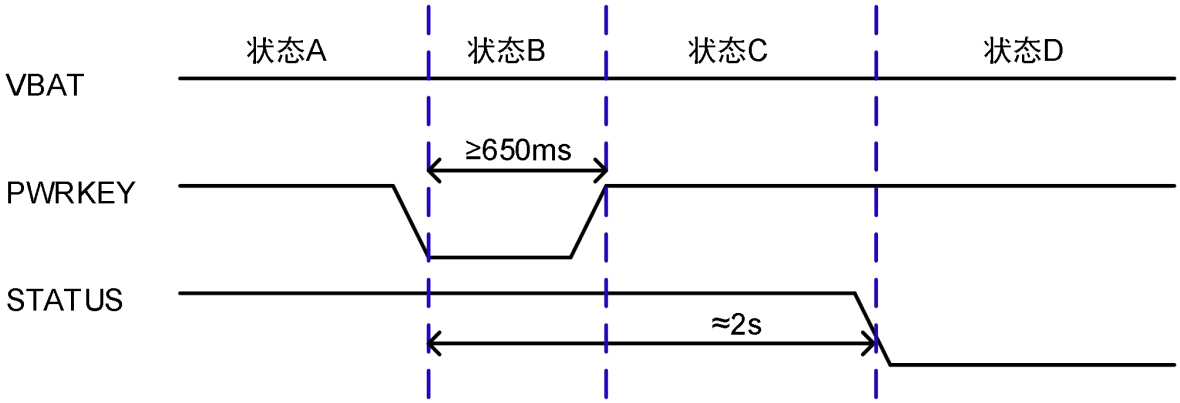
Notes:

◆ If you need to power on automatically and do not need the shutdown function, you can pull PWRKEY directly to ground. It is recommended to choose a pull-down resistor of 4.7kΩ, or control PWRKEY to a low level with GPIO before powering on the module and keep it that way.

◆ The main serial port of the module sends the character "Lierda", which indicates that the boot process is completed.

3.5.4 Shutdown sequence

When the power is on, pull down PWRKEY for 650ms and then release it, the module will execute the shutdown process, the timing is as follows:



PWRKEY shutdown timing description:

◆ Status A: Module operating status;

◆ Status B: Pull down the state of PERKEY for at least 650ms;

◆ Status C: The system shuts down inside the module, from pulling PWRKEY low to complete shutdown takes about 2 seconds;

◆ Status D: The module has entered shutdown mode.

3.6 Reset

3.6.1 Reset introduction

The RESET_N pin can be used for module reset. Pull down the RESET_N pin for at least 300ms and then release it to reset the module. The description of the RESET_N pin is as follows:

Table 3-4 Reset Pin Description

Pin number	Pin name	I/O	Description	DC characteristics	Note
15	RESET_N	DI	Module reset/shutdown	VILmax=0.45V	There is weak pull-up internally, low level effective, leave floating if not used.

3.6.2 Reset circuit reference design

The RESET_N signal is sensitive to interference. It is recommended that the module interface wiring should be as short as possible and should be grounded. Typical hardware circuit reference applications are as follows, and two circuit diagrams can be selected according to actual needs:

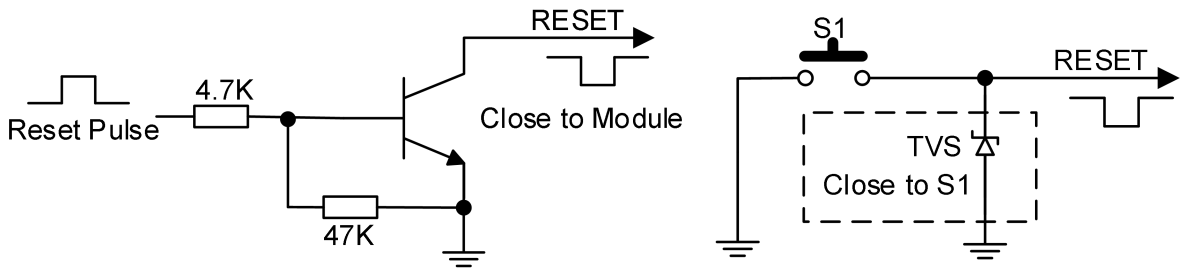
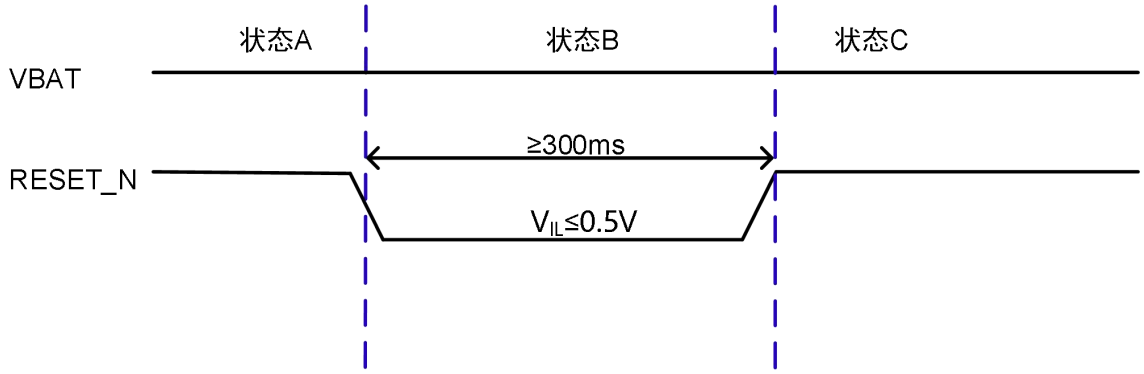


Figure 3.12 Reset Circuit Reference Design

3.6.3 Reset timing

The reset timing sequence of the module is as follows:



Reset timing description:

- Status A: Module in normal working condition;
- Status B: Pull down the RESET_N state for at least 300ms;
- Status C: Module starts rebooting.

4 Application interface

NT26-FEU D module provides rich peripheral functions, mainly including the following application interfaces:

- ◆ USB 2.0 Interface
- ◆ UART Interface
- ◆ USIM Interface
- ◆ I2C interface
- ◆ PCM interface
- ◆ CAMERA Interface
- ◆ LCD interface, etc.

4.1 USB interface

NT26-FEU D module supports USB2.0 interface, compliant with USB2.0 specification, supporting Full-Speed (12 Mbps) and High-Speed (480 Mbps) modes. The module only supports USB slave mode. This interface can be used for AT command sending, data transmission, software debugging, and firmware upgrade. The interface definition is as follows:

Table 4-1 USB Interface Pin Description

Pin number	Pin name	I/O	Description	DC characteristics	Note
59	USB_DP	DIO	USB differential data (+)	-	If not used, leave floating
60	USB_DM	DIO	USB differential data (-)	-	If not used, leave floating
61	USB_VBUS	DI	Sleep wakefulness	VDD18AON	In sleep mode, inserting USB will wake up the

					module;
82	USB_BOOT	DI	USB mode configuration interface	VO_LDOIO	Internal weak pull-down, leave floating if not used.

4.1.1 USB circuit reference design

The module USB interface can be connected to the USB connector or the MCU's USB interface. The reference schematic for connecting to the USB connector is as follows:

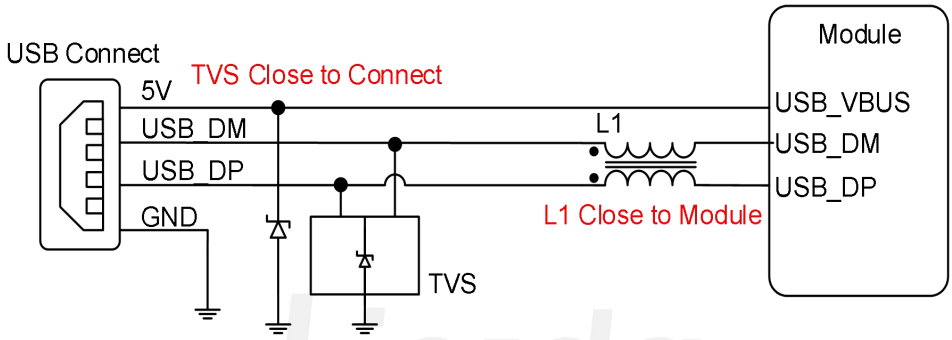


Figure 4.1 USB Interface Reference Design

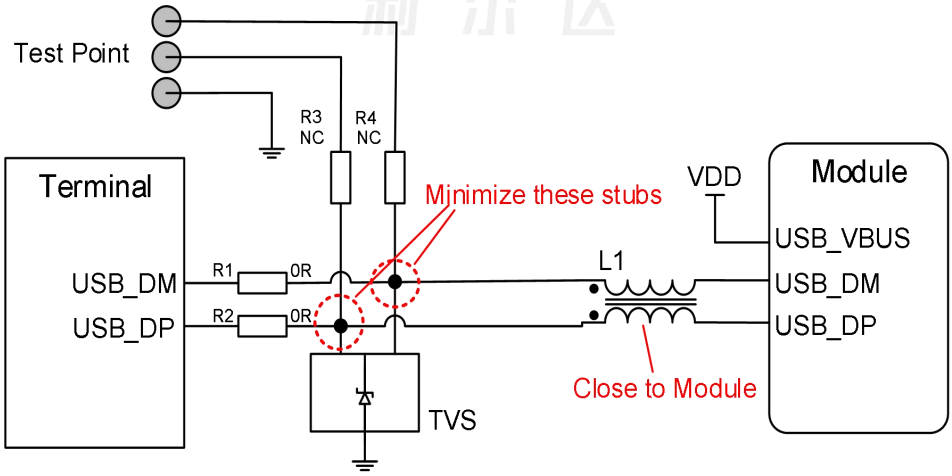


Figure 4.2 USB Connection MCU Reference Design

Notes:

◆ To ensure the performance of USB, the USB_DP and USB_DM traces should maintain a differential impedance of 90Ω, and proper grounding treatment is needed around them. It is recommended to add a common mode inductor L1 in series between the

MCU and the module to prevent USB signal from generating EMI interference, and L1 should be placed close to the module.

◆ USB traces should be kept away from crystal oscillators, oscillators, magnetic devices, RF signals, and strong signal areas. It is recommended to use inner layer differential traces and surround them with ground planes on all sides.

◆ If the USB interface of the module is connected to the MCU through a connector, a TVS tube protection should be added at the interface. Special attention should be paid to the selection of ESD protection devices, and the parasitic capacitance should not exceed 2pF, and they should be placed as close to the USB interface as possible.

◆ Reserve resistors R1~R5, normally solder R1, R2, and R5, do not solder R3 and R4 to connect to the MCU. When debugging is needed, solder R3 and R4, and do not solder R1 and R2 to switch to the test point. To meet the USB data signal integrity requirements, keep the bifurcation lines connecting to the test points as short as possible.

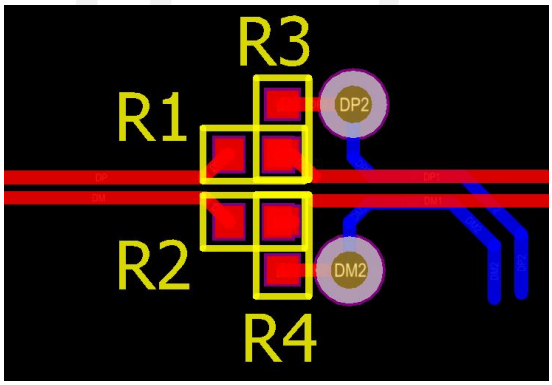


Figure 4.3 USB jumper wiring diagram

4.1.2 USB data transfer

When the module is powered on or reset, if USB_BOOT is detected as a low level, the USB port will enumerate 2 serial ports for AT command sending and log output.

4.1.3 USB firmware download

When the module is powered on or reset, if USB_BOOT is detected as a high level, the

USB port will enumerate a dedicated serial port for downloading. At this time, the download tool can upgrade the firmware through the USB interface. If there is no connection to the download tool for more than 15 seconds, the module will re-enumerate 2 serial ports according to the normal USB configuration.

USB_BOOT interface reference design is as follows:

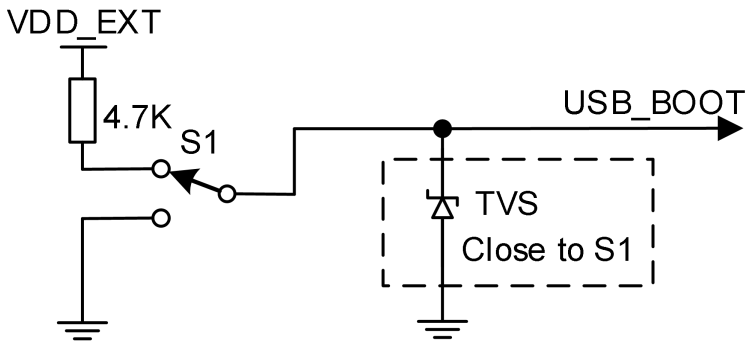


Figure 4.4 USB_BOOT Reference Design

4.2 UART communication

The module provides 3 general asynchronous transceivers: main serial port, debug serial port, and auxiliary serial port. The baud rate of the main serial port is configurable, and the debug serial port is only used for debugging and testing. The serial port pin definitions are as follows:

Table 4-2 Serial Port Pin Definitions

Interface	Pin number	Pin name	Description	Note
Main serial port	17	MAIN_RXD	Main serial port receives data	Non-sleep mode: VDD_EXT power domain; Sleep mode: Switch to internal AON power domain
	18	MAIN_TXD	Main serial port sends data	If not used, leave floating

	19	MAIN_DTR	Main serial port data terminal ready	In sleep mode, the wake-up pin can be used.
	20	MAIN_RI	Main serial port outputs ringing prompt.	If not used, leave floating
	21	MAIN_DCD	Main serial port output carrier detection	If not used, leave floating
	23	MAIN_CTS	Main serial port DTE clear to send	Connect CTS to DTE, leave floating if not used.
	22	MAIN_RTS	Main serial port DTE requests transmission.	Connect RTS to DTE, leave floating if not used.
Debugging serial port	38	DBG_RXD	Debugging serial port receiving data	If not used, leave floating
	39	DBG_TXD	Debug serial port data transmission	If not used, leave floating
Auxiliary serial port	28	AUX_RXD	Assist in receiving data through the serial port.	Not supported temporarily
	29	AUX_TXD	Assist in sending data through the serial port.	Not supported temporarily

Precautions:

◆ The serial port interface belongs to the VO_LDOIO power domain, and the maximum voltage should not exceed 3.6V;

◆ VO_LDOIO power domain will power off in sleep mode, MAIN_RXD switches to internal 1.2V power supply;

◆ The serial port RXD pin has an internal pull-up and does not require an external pull-up resistor to be connected;

◆ Pay attention to the consistency of the voltage levels when using the serial port, otherwise it may easily generate leakage current.

4.2.1 Serial port application

Main serial port characteristics:

◆ Used for AT command communication and data transmission, default baud rate is 115200bps;

◆ Configurable as: 4800/9600/19200/38400/57600/115200/230400/460800bps;

◆ Used for firmware upgrade, the default baud rate is 921600bps during the upgrade;

◆ Supports low power consumption wake-up module function.

Debugging serial port characteristics:

◆ Through the dedicated tools provided by the platform, you can view log information for software debugging, defaulting to 3000000bps.

Serial port connection diagram is as follows:

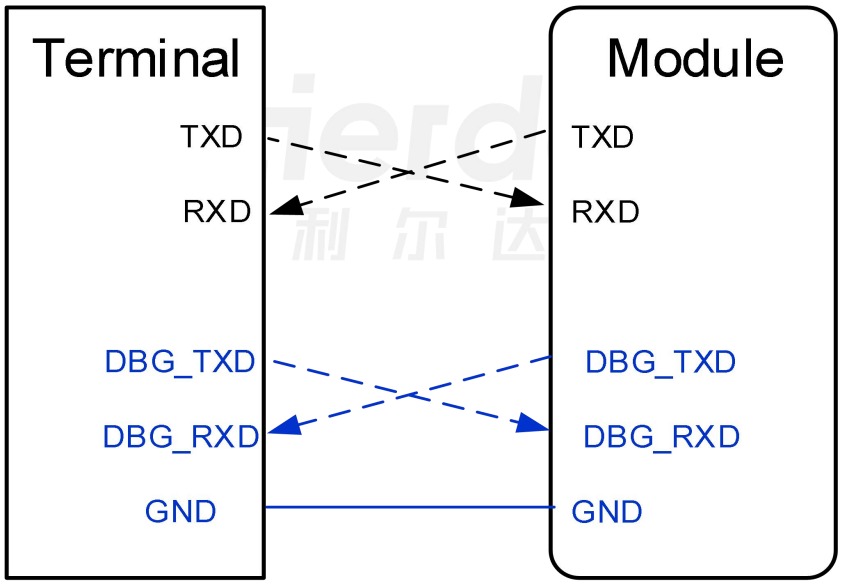


Figure 4.5 Serial Port Connection Diagram

4.2.2 Serial port circuit reference design

The main factors to consider in a suitable serial port level conversion circuit are whether it meets the working speed of the serial port, scenarios with low power requirements, and whether the power consumption meets the requirements. It is recommended to refer to the following level matching circuit:

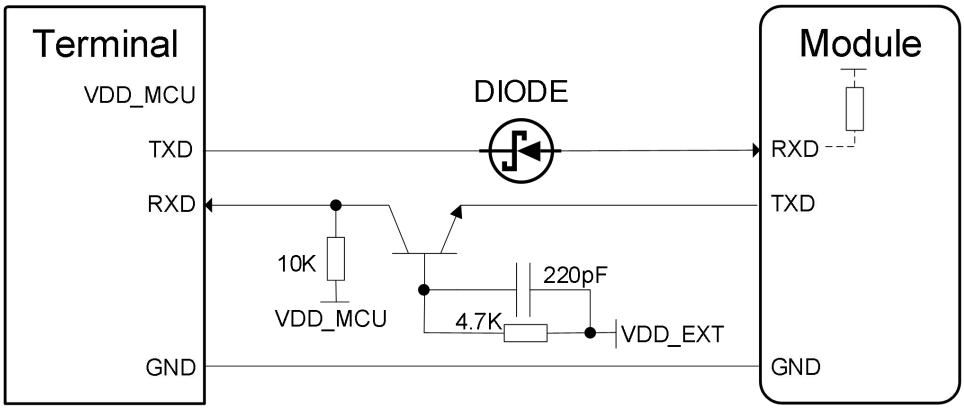


Figure 4.6 Transistor Level Conversion Reference Circuit

Recommended transistor, for reference:

Brand: CJ Specifications: S8050 J3Y Package: SOT-23

Recommended diode, pay attention to the forward voltage of the diode ≤0.3V, for reference:

Brand: LRC Model: LRB520S-30T1G Package: SOD-523

4.3 USIM card interface

The module includes an external USIM card interface, compliant with ETSI and IMT-2000 specifications, supporting 1.8V and 3.0V USIM cards. The pin descriptions are as follows:

Table 4-3 Definition of External USIM Card Interface Pins

Pin number	Pin name	Description	DC Characteristics
11	USIM_DATA	SIM card data cable	VO_LDOSIM
12	USIM_RST	SIM card reset line	VO_LDOSIM
13	USIM_CLK	SIM card clock line	VO_LDOSIM
15	USIM_VDD	SIM card power supply	Vnorm=1.8/3.0V
91	USIM_DET	SIM card status signal detection	SIM card slot hot plug detection interface
62	USIM2_CLK	SIM card 2 clock line	VO_LDOIO
63	USIM2_RST	SIM card 2 reset line	VO_LDOIO
64	USIM2_DATA	SIM card 2 data cable	VO_LDOIO
65	USIM2_VDD	SIM card 2 power	Same power supply as USIM_VDD

The module supports hot-swappable detection of USIM cards through USIM_DET, with this function enabled by default, supporting high/low level detection. If not used, leave USIM_DET floating.

4.3.1 USIM card circuit reference design

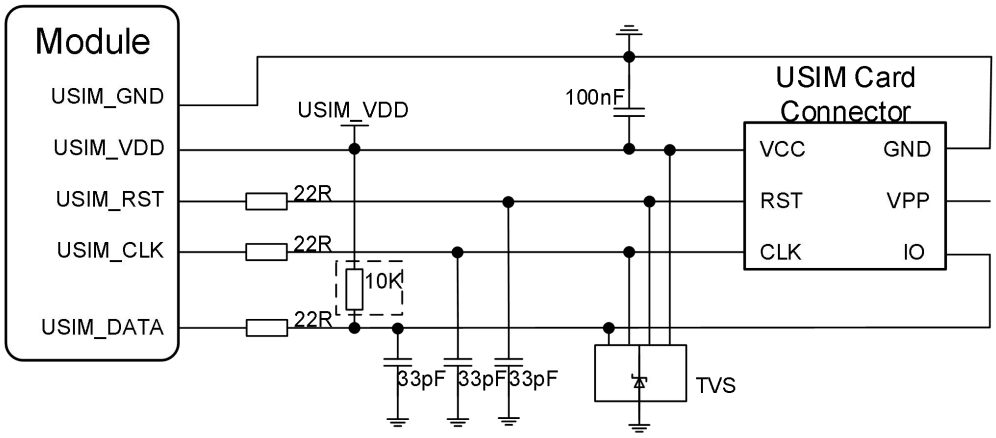


Figure 4.7 6PIN SIM card reference circuit

4.3.2 Considerations for USIM card circuit design

To ensure the reliability and availability of SIM card in applications, please follow the following USIM circuit design guidelines:

◆ When laying out, try to place the SIM card close to the module, and keep the signal line wiring length within 200mm if possible;

◆ SIM card signal line away from RF traces and VBAT power line;

◆ The GND wiring of the SIM card should be short and thick, ensuring that the wiring width is not less than 0.5mm;

◆ The decoupling capacitance of USIM_VDD should not exceed 1uF, and the capacitance should be placed close to the VCC of the external SIM card.

◆ In order to avoid signal interference between USIM_DATA and USIM_CLK, the wiring between the two should not be too close. Ground shielding should be added between the two lines. In order to avoid the impact of long lines, USIM_DATA generally needs to add a pull-up resistor to USIM_VDD to improve the driving capability. If the lines are too long, it is recommended to externally reserve a 10K resistor near the card slot. In addition, the USIM_RST signal also needs to be ground protected.

◆ To ensure good ESD protection performance, it is recommended to add a TVS

diode to the external USIM card's pins. The parasitic capacitance of the selected TVS diode should not exceed 15pF; a 22-ohm resistor should be connected in series between the signal lines of the module and the SIM card to suppress stray EMI and enhance ESD protection. Additionally, a parallel 33pF capacitor should be used to filter out RF interference. The relevant resistors, capacitors, and TVS diode should be placed near the USIM card slot.

4.4 I2C Interface

The module provides 1 I2C interface, and the interface description is as follows:

Table 4-4 I2C Interface Pin Definitions

Pin number	Pin name	Description	DC characteristics	Note
66	I2C_SDA	I2C data	VO_LDOIO	External pull-up required
67	I2C_SCL	I2C clock	VO_LDOIO	External pull-up needed

Notes:

◆ It is recommended to use a 4.7K resistor for pull-up on the data line and clock line of I2C.

4.5 PCM interface

4.5.1 Introduction to PCM

The module provides 1 PCM interface, and the interface description is as follows:

Table 4-5 PCM Interface Pin Definitions

Pin number	Pin name	Description	DC characteristics	Note
30	PCM_CLK	PCM clock output	VO_LDOIO	

31	PCM_SYNC	PCM synchronization signal	VO_LDOIO	
32	PCM_DIN	PCM data input	VO_LDOIO	
33	PCM_DOUT	PCM data output	VO_LDOIO	
26	PCM_MCLK	PCM reference master clock	VO_LDOIO	

4.5.2 Codec reference application

Codec function can be achieved through PCM and I2C of the module, the common application reference circuit is as follows:

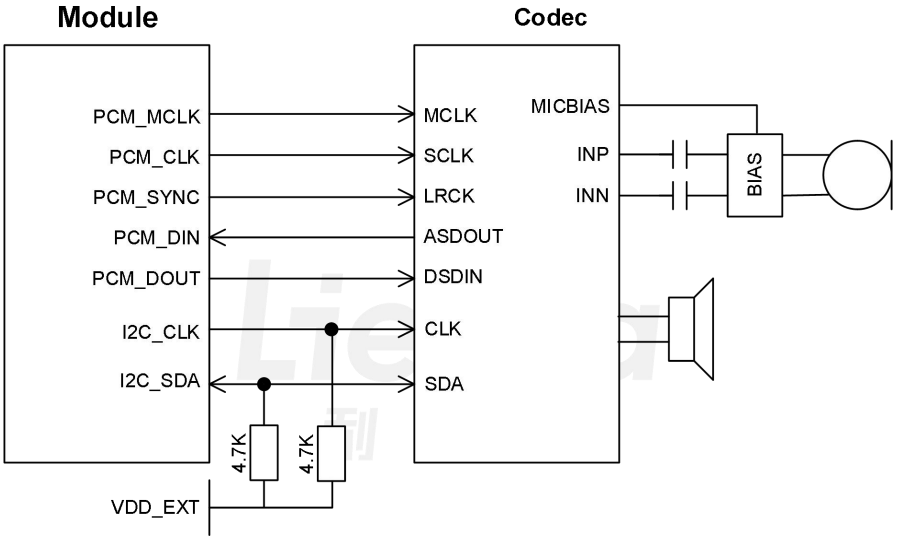


Figure 4.8 Codec Application Reference Circuit

The document "Lierda NT26-FEU D Series Hardware Reference Design Manual" for the module provides various Codec solutions for users to choose according to their actual needs.

4.6 SPI and LCD interface

4.6.1 Interface introduction

The module provides 1 set of SPI-based LCD interface, PIN[50..53] is a standard SPI interface, combined with other pins, can also be reused for LCD function, the interface description is as follows:

Table 4-7 SPI Interface Pin Definitions

Pin number	Pin name	Description	DC characteristics	Note
49	LCD_RST	DO	LCD reset	VO_LDOIO
50	LCD_SIO	DIO	LCD data output	VO_LDOIO
51	LCD_SDC	DO	LCD data address switch signal	VO_LDOIO
52	LCD_CS	DO	LCD chip selection	VO_LDOIO
53	LCD_CLK	DO	LCD clock	VO_LDOIO
78	LCD_TE	DI	LCD frame synchronization	LDO_AONIO

4.6.2 SPI Reference Application

The SPI of the module can be used as a master device or as a slave device. The application reference circuit is as follows:

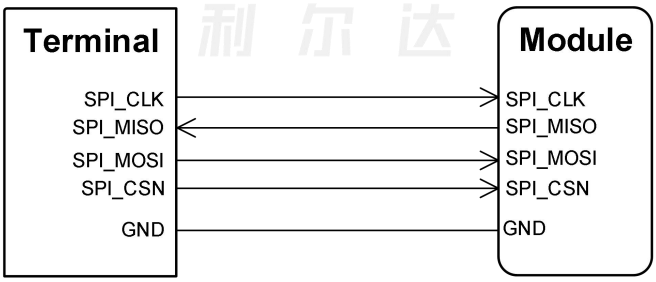


Figure 4.10 SPI Interface Circuit Reference Design (Module as Slave Device)

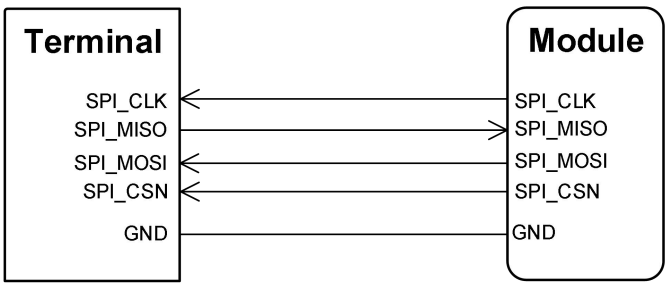


Figure 4.11 SPI Interface Circuit Reference Design (Module as Master Device)

4.6.3 LCD reference application

The LCD function of the module, the actual circuit will vary depending on the selected

LCD, please refer to the "Lierda NT26-FEU D Series Hardware Reference Design Manual" for specific circuit details.

4.7 Camera interface

4.7.1 Interface introduction

The module provides a set of camera interfaces based on SPI and I2C, supporting up to 30-megapixel sensors, and allowing SPI single data line or dual data line transmission. The interface details are as follows:

Table 4-8 Camera Interface Pin Definitions

Pin number	Pin name	Description	DC characteristics	Note
8	CAM_VDD*	Camera power supply	VO_LDOIO	The pin module can be configured as CAM_VDD by selecting and pasting the reserved circuit internally.
54	CAM_MCLK	Camera main clock	VO_LDOIO	If not used, leave floating
55	CAM_DATA0	Camera data is D0.	VO_LDOIO	If not used, leave floating
56	CAM_DATA1	Camera data is D1.	VO_LDOIO	If not used, leave floating
57	CAM_I2C_SCL	Camera I2C clock	VO_LDOIO	If not used, leave floating, external pull-up is needed when in use.
58	CAM_I2C_SDA	Camera I2C data	VO_LDOIO	If not used, leave floating, external pull-up is needed when in use
80	CAM_SPI_CLK	Camera SPI clock	VO_LDOIO	If not used, leave floating

81	CAM_PWDN	Camera off	VO_LDOIO	If not used, leave floating
103	CAM_RST_N	Camera reset	VO_LDOIO	If not used, leave floating

Note:

If the customer needs to power the camera with CAM_VDD, the following two solutions can be modified:

◆ Modify VO_LDOIO to 2.8V through software.

◆ The module hardware reserves a 2.8V LDO (not currently mounted), you can contact Lierda to obtain this version of the module.

4.7.2 Camera reference application

The camera function of the module, the actual circuit will vary depending on the selected camera, please refer to the specific circuit in the "Lierda NT26-FEU D Series Hardware Reference Design Manual" document.

4.8 ADC interface

The module provides 2 12-bit analog-to-digital conversion input interfaces (ADC interfaces). When wiring the ADC interfaces, in order to improve the voltage measurement accuracy of the interfaces, it is recommended to perform grounding treatment. The pin definitions are as follows:

Table 4-9 ADC Pin Definitions

Pin number	Pin name	Description	DC characteristics	Note
9	ADC0	ADC0 interface	Internal direct connection Input voltage range: 0~1.6V Internal partial pressure Input voltage range: 0~3.3V	The effective input voltage range for internal direct connection is 0.1V to 1.5V, there may be
96	ADC1	ADC1 Interface		

			Default 1.6V Internal partial pressure can be activated through the software.	significant errors in the range of 0V to 0.1V and 1.5V to 1.6V, so it is not recommended to use.

Precautions:

◆ If the collected voltage is greater than 3.3V, it is recommended to use a resistor divider circuit input for the ADC pin. The resistance value of the divider resistor should not exceed 100kΩ, otherwise it will reduce the measurement accuracy of the ADC.

◆ When designing, leave a 1nF capacitor at both ends of the grounding voltage divider resistor, do not solder by default.

4.9 Status indication signal

The module has one network status indicator and one operation status indicator interface, the interface is defined as follows:

Table 4-10 Status Indicator Pin Definitions

Pin number	Pin name	Description	DC Characteristics	Note
16	NET_STATUS	Network status indicator	VDD18AON	If not used, leave floating
25	STATUS	Operating status indication	VDD18AON	If not used, leave floating

4.9.1 Indicator light circuit reference design

NET_STATUS pin is used to indicate the network status of the module. The logic levels under different statuses are as follows:

Table 4-11 Status Indicator Pin Definitions

Pin name	Logic level	Network status
NET_STATUS	Slow flash (200ms high / 1800ms low)	Search network status
	Slow flash (1800ms high/200ms low)	Standby mode
	Quick flash (125ms high/125ms low)	Data transmission mode

4.9.2 Operating status indication

The STATUS pin is used to indicate the operating status of the module. When the module is powered on normally, STATUS will output a high level, and it remains valid even in sleep mode.

4.9.3 Indicator light circuit reference design

NET_STATUS and STATUS pins can both be used to drive LED indicator lights, the reference design is as follows:

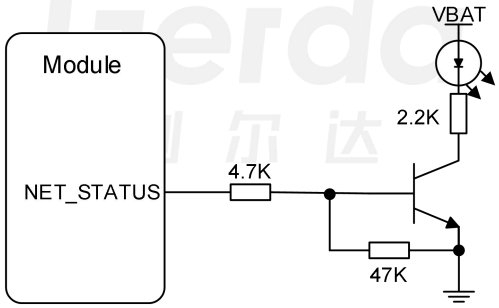


Figure 4.12 Indicator Light Reference Circuit

5 RF characteristics

5.1 Introduction to RF Function

NT26-FEU D module provides a main antenna RF interface, all air interface data is

sent or received from this interface, and the interface impedance is 50Ω. Interface description is as follows:

Table 5-1 RF Interface Pin Definitions

Pin number	Pin name	I/O	Description	DC characteristics	Note
35	ANT_MAIN	AIO	Main antenna interface	-	Used for air interface data transmission

5.2 Cellular network

5.2.1 Working frequency band

NT26-FEU D module supports the following operating frequency bands:

Table 5-2 Working Frequency Bands

Frequency band Band	Uplink frequency band Uplink(UL)band	Downlink frequency band Downlink(DL)band	Network standard Duplex Mode
1	1920MHz-1980MHz	2110MHz-2170MHz	FDD
3	1710MHz-1785MHz	1805MHz-1880MHz	FDD
5	824MHz-849MHz	869MHz-894MHz	FDD
7	2500MHz-2570MHz	2620MHz-2690MHz	FDD
8	880MHz-915MHz	925MHz-960MHz	FDD
20	832MHz-862MHz	791MHz-821MHz	FDD
28	703MHz-748MHz	758MHz-803MHz	FDD
38	2570MHz-2620MHz	2570MHz-2620MHz	TDD
40	2300MHz-2400MHz	2300MHz-2400MHz	TDD
41	2496MHz-2690MHz	2496MHz-2690MHz	TDD

5.2.2 Transmit power

The transmission power of the NT26-FEU D module is as follows:

Table 5-3 Conduction Power

Band	Network standard	Maximum value	Minimum value	Note
1	FDD	23dBm±2.7dB	＜-40dBm	Compliant with Cat.1 protocol in 3GPP Rel-13 and Rel-14.
3	FDD	23dBm±2.7dB	＜-40dBm	
5	FDD	23dBm±2.7dB	＜-40dBm	
7	FDD	23dBm±2.7dB	＜-40dBm	
8	FDD	23dBm±2.7dB	＜-40dBm	
20	FDD	23dBm±2.7dB	＜-40dBm	
28	FDD	23dBm±2.7dB	＜-40dBm	
38	TDD	23dBm±2.7dB	＜-40dBm	
40	TDD	23dBm±2.7dB	＜-40dBm	
41	TDD	23dBm±2.7dB	＜-40dBm	

5.2.3 Receive sensitivity

The receiving sensitivity of the NT26-FEU D module is as follows:

Table 5-4 Conduction reception sensitivity under single transmission (throughput ≥ 95%)

Band	Network standard	Sensitivity (10M)	3GPP standard (10M)
1	FDD	-98.8	-96.3dBm
3	FDD	-98.3	-93.3dBm
5	FDD	-99.3	-94.3dBm
7	FDD	-98.2	-94.3dBm
8	FDD	-98.5	-93.3dBm

20	FDD	-98.8	-93.3dBm
28	FDD	-98.4	-94.8dBm
38	TDD	-98.5	-96.3dBm
40	TDD	-99.3	-96.3dBm
41	TDD	-98	-94.3dBm

5.3 Antenna reference circuit design

When users use the NT26-FEU D module, a π-type matching circuit needs to be added between the RF antenna interface of the module and the antenna interface of the user's baseboard. The typical antenna matching circuit and initial parameters are shown in the figure below:

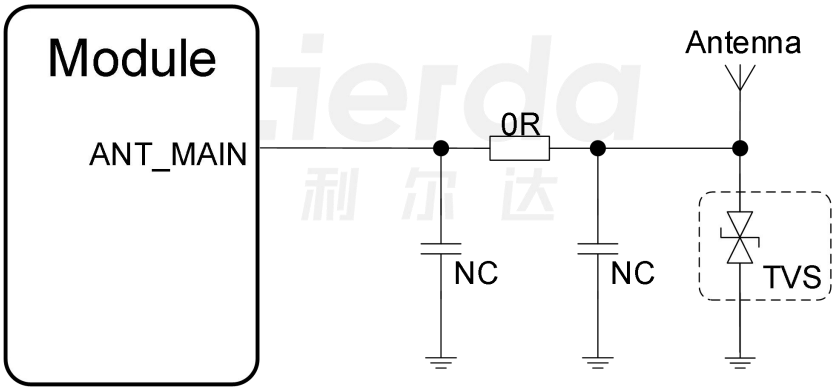


Figure 5.1 RF Antenna Reference Circuit

Notes:

◆ The resistor is set to 0 ohms, the capacitor position is not populated by default, and it is recommended to use 0201 or 0402 package for the component package.

◆ If an external antenna is used, or if users can touch the antenna, it is recommended to reserve a TVS tube to enhance electrostatic protection. Because the parasitic capacitance of the TVS may affect the antenna performance, it is recommended to re-adjust the antenna after adding the TVS tube.

5.4 RF signal line wiring guide

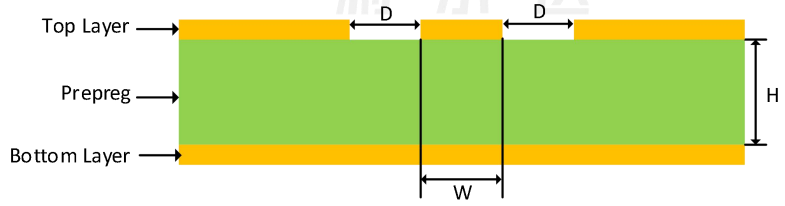
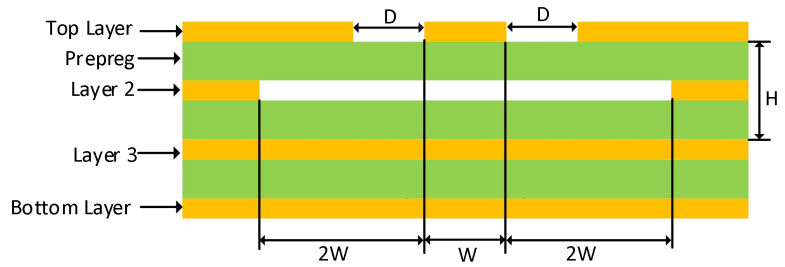
The routing between the module antenna interface and the user antenna must meet the 50-ohm characteristic impedance requirement, and the RF routing should be as short as possible to ensure minimal insertion loss of the RF routing.

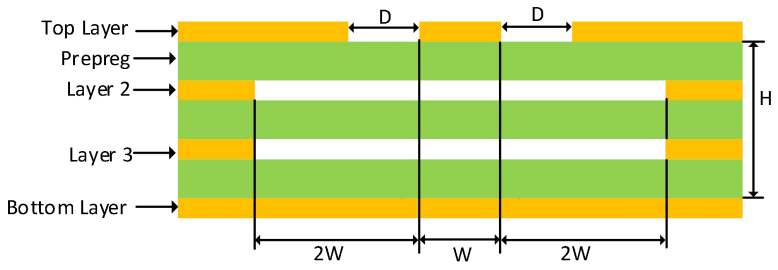
In general, the impedance of the RF signal line is determined by the material's dielectric constant Er, the trace width W, the spacing to the ground D, and the thickness of the reference ground plane H.

In the field of IoT applications, the design of PCB characteristic impedance typically adopts the coplanar waveguide method, which helps to achieve better shielding for RF signal lines, while also enabling higher integration for small area designs.

Common PCB coplanar waveguide designs include the following:

Table 5-5 Description of Common PCB Coplanar Waveguide Structures

Serial Number	Pin name	Note
1		2-layer board Reference ground is at Layer 2.
2		4-layer board Reference level is L3. Digging a hole at layer 2

3		4-layer board Reference ground is at level L3. Digging holes on floors L2 and L3.

During the Layout process, 50 ohm impedance can be simulated and calculated using the Polar Si9000 tool. According to the actual situation, choose the appropriate line width, spacing, and stackup to achieve the best design effect.

Using a 2-layer PCB with a thickness of 1.6mm as an example to calculate the coplanar waveguide.

◆ Choose the appropriate PCB material, once the material is selected, the dielectric constant Er is basically determined (in this case, it is 4.6);

◆ Choose the appropriate line width, a good method is to select a line width that matches the size of the pad left with the device (note that it cannot be too thin, choose 0.65mm in this example);

◆ Based on the selected board thickness, line width, dielectric constant, etc., the spacing to ground can be roughly calculated. If the line spacing is not appropriate, the line width can be adjusted to adjust the line spacing (calculated to be 0.14mm, which is basically suitable).

Figure 5.2 Reference for calculating 50 ohm impedance.

In the actual layout process, the following suggestions are for reference:

◆ Three matching reserved components in the π-type circuit are placed closely near the antenna, and bypass components are recommended to be placed on both sides of the RF line.

◆ Irregular vias are placed on both sides of the RF trace GND plane, and there must be a complete GND plane below the entire RF trace space;

◆ There should be no other traces below the RF line to avoid affecting the RF performance or other circuits.

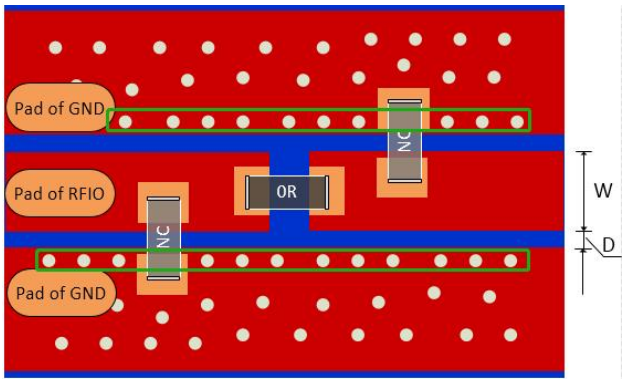


Figure 5-3 RF routing LAYOUT design schematic

The rationality of RF routing can be directly reflected in the conduction test of the module. In order to ensure the full performance of the product, antenna design cooperation is also required. In order to better meet the requirements of antenna design, the following requirements are hoped to be achieved in PCB design. Guidance is provided below for different layers of the whole PCB.

◆ When the product PCB is designed with 2 layers, it is best for the TOP and BOTTOM LAYER directly below the module to be GND layers. The traces that need to be led out of the module should avoid running directly below the module and should be led out from the outer side of the module.

◆ When the product PCB is designed as a 4-layer board, it is recommended that the traces to be routed for the module should be on the third or fourth layer, while reserving the

first and second layers as complete GND reference layers for the module.

5.5 Antenna design requirements

The RF performance of the module is also affected by the antenna. The selection of the antenna needs to meet the following requirements:

◆ Choose an antenna that matches the operating frequency band of the module;

◆ Request the characteristic impedance of the antenna to be 50 ohms, reduce the loss at the connection between the RF cable and the antenna;

◆ The smaller the insertion loss within the working frequency band, the better, such as VSWR ≤ 2, return loss ≥ 10dB, etc.;

The commonly used antenna suitable for Cat.1 scenarios is as shown in the following figure:

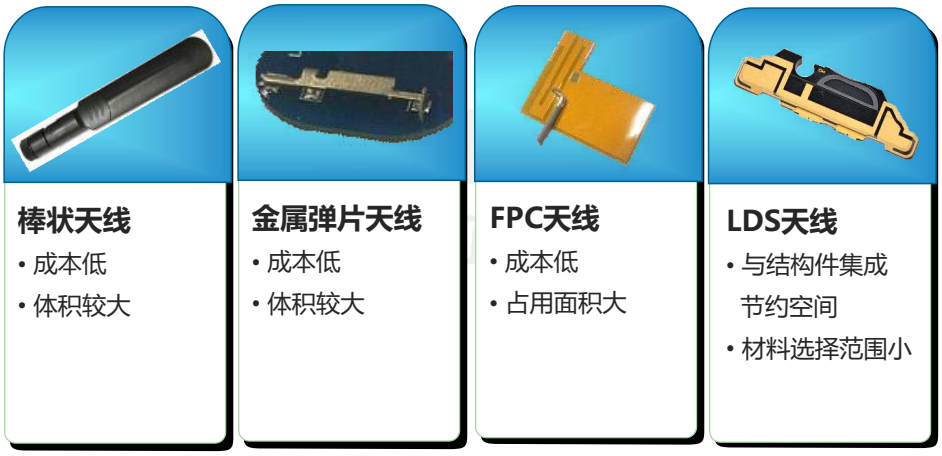


Figure 5.4 Commonly used antenna types for Category 1.

5.6 RF connector recommendation

In some applications that require customized antennas, such as in environments where devices are shielded by metal casing, an IPX or SMA connector can be left on the motherboard to connect the antenna outside the device through a RF cable to achieve better performance.

Table 5.6 Common RF Connectors

Serial number	Product Name	Image	Note
1	IPX seat		RF feedline
2	SMA seat		Can connect to RF cable or antenna

6 Electrical performance and reliability

6.1 Absolute maximum rated value

The absolute maximum rated value description of the NT26-FEU D module interface is as follows:

Table 6-1 Absolute Maximum Ratings

Parameters	Description	Minimum value	Maximum value	Unit	Note
VBAT	Module power supply voltage	-0.3	5.0	V	
VI_{AIO}	ADC input voltage	-0.3	3.6	V	
VI_{GPIO}	GPIO input voltage	-0.3	3.6	V	
Others	Other pin input voltage	-0.3	3.6	V	

Note: Exceeding the absolute maximum rated value may cause permanent damage to the module.

6.2 Rated power value

The electrical characteristics of the NT26-FEU D module power interface are described as follows:

Table 6-2 Electrical Characteristics of Power Interface

Parameters	Description	Minimum value	Typical value	Maximum value	Unit
VBAT	Power supply input for the module	3.3	3.8	4.5	V
USIM_VDD	USIM card power supply output	-	1.8/3.0	-	V
VDD_EXT	Reference power output	-	1.8	-	V
CAM_VDD	Camera power supply	-	1.8	-	V

Note: VDD_EXT and CAM_VDD are default powered off in sleep mode.

6.3 Power consumption

Power consumption of NT26-FEU D module is as follows:

Table 6-3 Module Power Consumption

Module description	Test conditions	Typical value	Unit
Shutdown mode	Module shutdown	0.9	uA
Sleep mode	AT+CFUN=0 (USB disconnected)	2.6	uA
	LTE-FDD @ PF = 32 (USB disconnected)	0.63	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.34	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.21	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.15	mA
	LTE-TDD @ PF = 32 (USB disconnected)	0.67	mA
	LTE-TDD @ PF = 64 (USB disconnected)	0.36	mA
	LTE-TDD @ PF = 128 (USB disconnected)	0.21	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.16	mA
Idle mode	LTE-FDD @ PF = 64 (USB disconnected)	3.27	mA
	LTE-FDD @ PF = 64 (USB connection)	TBD	mA
	LTE-TDD @ PF = 64 (USB disconnected)	3.91	mA
	LTE-TDD @ PF = 64 (USB connection)	TBD	mA
LTE data transmission	LTE-FDD B1	579	mA
	LTE-FDD B3	647	mA
	LTE-FDD B5	466	mA
	LTE-FDD B7	520	mA
	LTE-FDD B8	469	mA
	LTE-FDD B20	483	mA
	LTE-FDD B28	568	mA
	LTE-TDD B38	183	mA
	LTE-TDD B40	191	mA
	LTE-TDD B41	184	mA

6.4 Digital logic voltage characteristics

The GPIO logic level definition of the NT26-FEU D module is as follows:

Table 6-4 Explanation of Digital IO Logic Levels

Type	Parameters	Description	Minimum value	Maximum value	Unit
Enter	VIL	Enter low level	-	0.2*VDD_EXT	V
	VIH	Input high level	0.7*VDD_EXT	-	V
Output	VOL	Output low level.	-	0.15*VDD_EXT	V
	VOH	Output high level	0.8*VDD_EXT	-	V

Note: The GPIO level of the module follows VDD_EXT, and power will be lost during sleep.

The AGPIO logic level definition of the NT26-FEU D module is as follows: (AON_VDD range: 1.7~1.9V; typical value: 1.8V)

Table 6-4 Explanation of Digital IO Logic Levels

Type	Parameters	Description	Minimum value	Maximum value	Unit
Input	VIL	Enter low level	-	0.2*AON_VDD	V
	VIH	Input high level	0.7*AON_VDD	-	V
Output	VOL	Output low level	-	0.15*AON_VDD	V
	VOH	Output high level	0.8*AON_VDD	-	V

Note: The AGPIO reference level of the module is AON_VDD (internal reference voltage), and it will not lose power during sleep.

NT26-FEU D module USIM card interface logic level definitions are as follows:

Table 6-5 USIM Logic Level Description

Type	Parameters	Description	Minimum value	Maximum value	Unit
Input	VIL	Enter low level	-	0.2*USIM_VDD	V
	VIH	Input high level	0.7*USIM_VDD	-	V
Output	VOL	Output low level	-	0.15*USIM_VDD	V
	VOH	Output high level	0.8*USIM_VDD	-	V

Note: The voltage level of USIM_VDD will be determined based on the detected category of the USIM card, supporting 1.8/3.0V USIM cards.

6.5 Static electricity protection

Static electricity is everywhere in life and production. Static electricity generated by human body static electricity, object friction, etc., may be transferred to the module through various ways, and may cause damage to the module. Therefore, it is necessary to pay attention to static electricity protection and take static electricity protection measures. For example:

◆ Wear anti-static gloves during the research and development, production, assembly, and testing processes;

◆ When designing products, add anti-static protection devices at circuit interfaces and other points susceptible to electrostatic discharge.

The electrostatic discharge performance of the module is as follows:

Table 6-6 Electrostatic Protection Characteristics

Test interface	Discharge contact	Note
VBAT	±8KV	Test standard: IEC61000-4-2 Temperature: 25ºC Humidity: 45%
GND	±8KV	
Antenna interface	±8KV	

Other	-	

Static electricity protection detailed design reference "Lierda NT26-FEU D Series Hardware Reference Design Manual".

6.6 Working and storage temperature

Table 6-7 Working Temperature Range

Parameters	Minimum value	Typical value	Maximum value	Unit	Note
Normal operating temperature(1)	-35	+25	+75	℃	
Expand operating temperature(2)	-40	+25	+85	℃	
Storage environment temperature(3)	-40	+25	+90	℃	

Note (1): When the module operates within this temperature range, the module's relevant performance meets the 3GPP standard requirements.

Note (2): When the module operates within this temperature range, the module can still maintain normal operation without irreversible faults; only individual indicators, such as output power and other parameter values, may exceed the range of the 3GPP standard. When the temperature returns to the normal operating range, all indicators of the module still comply with the 3GPP standard.

Note (3): This storage temperature range does not include packaging materials. Please pay attention to the maximum temperature tolerance of the tape and reel packaging.

6.7 Precautions

Matters needing attention in the production and use of modules:

◆ When spraying the module, please try to avoid the spraying material flowing into the interior of the module;

◆ When cleaning the module, do not use ultrasonic cleaning on the module, as it may

cause damage to the internal crystals of the module.

◆ When producing and using modules, please avoid applying them in environments or packaging containing any amount of mercury or mercury vapor, as this may lead to the risk of product failure or malfunction.

7 Mechanical dimensions

7.1 Mechanical dimensions

Module mechanical dimension diagram as follows:

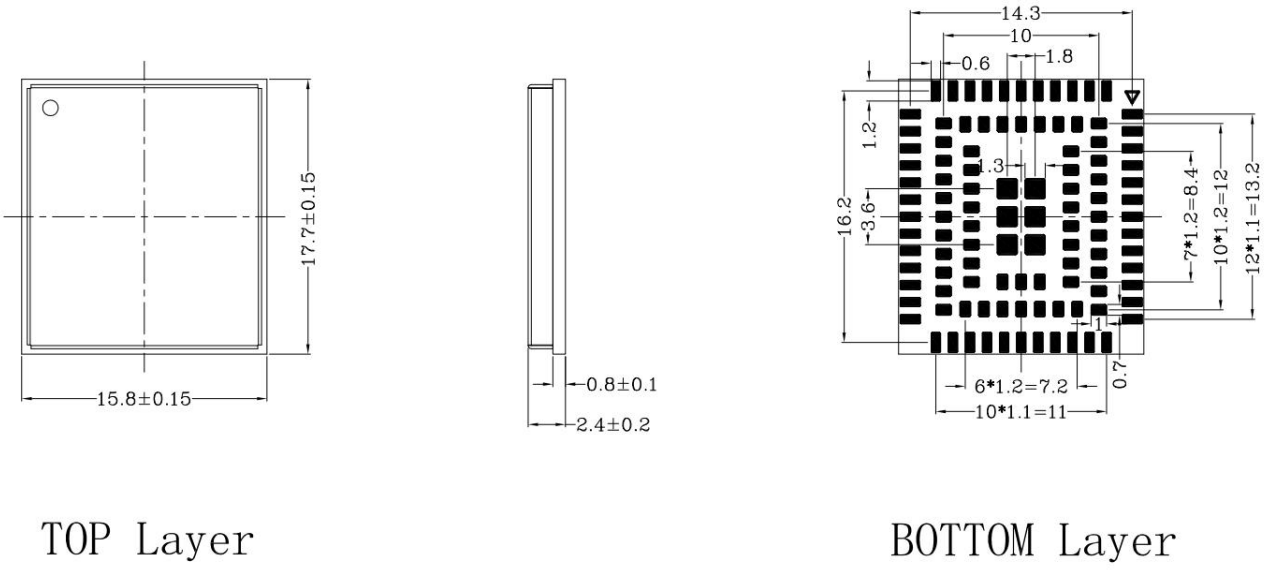


Figure 7.1 Module Mechanical Dimension Diagram

7.2 Module top view / bottom view

The module effect diagram is as follows, please refer to the actual module for specifics:

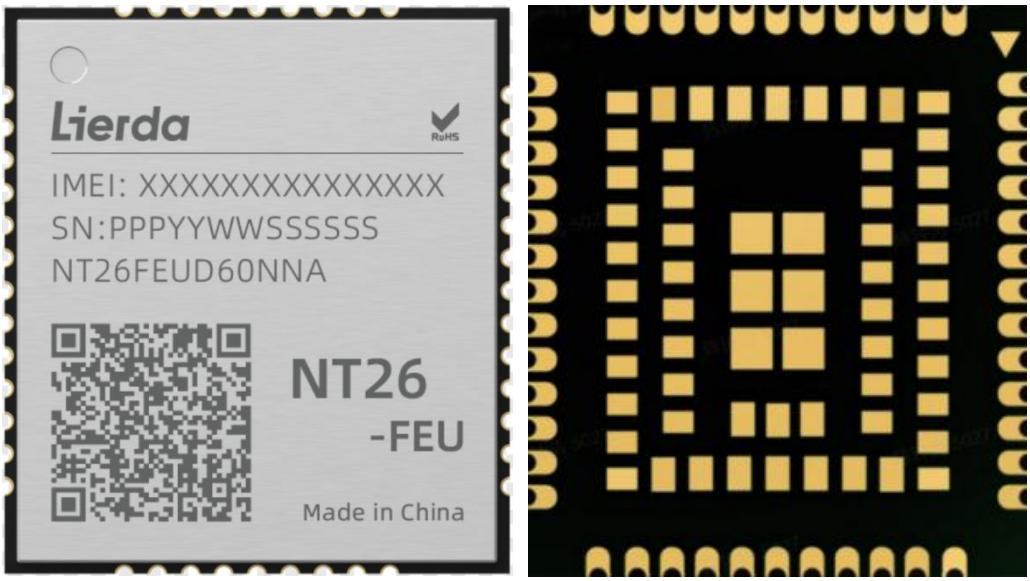


Figure 7.2 Module Top/Bottom View Diagram

7.3 Recommended encapsulation

The module recommends the solder pads as shown in the following figure, and users can make minor adjustments according to their own production processes.

◆ The pins around the module are designed with rounded corners internally. When designing the bottom board for soldering, please consider using rounded corners for transition. The rectangular solder pads at the bottom of the module can be designed using the module pin dimensions. Please refer to the design diagram of a single solder pad below.

◆ In order to facilitate the opening of the step steel mesh, it is recommended not to layout other components within 2.0mm range outside the module welding pad. Users can refer to the requirements of their own steel mesh manufacturers to determine this distance.

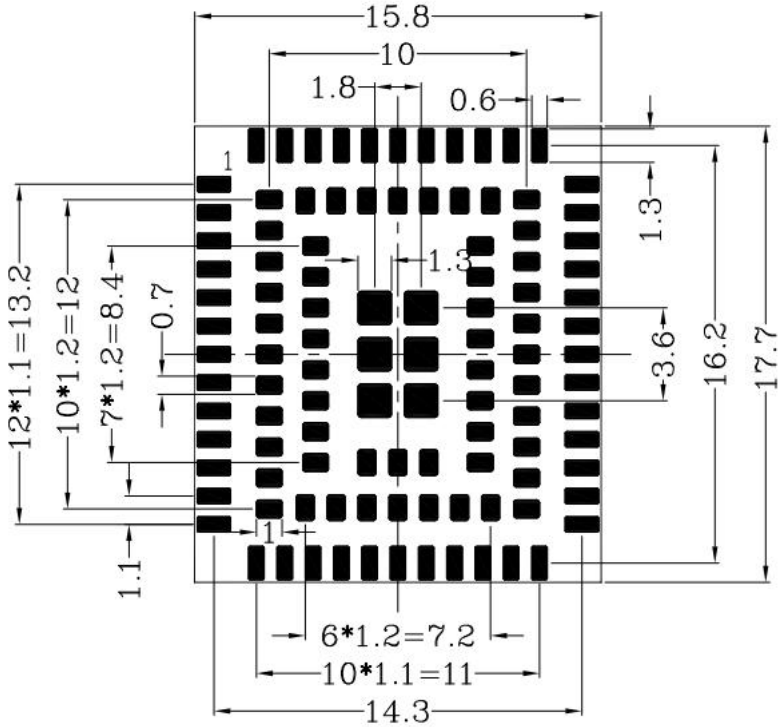


Figure 7.3 Module Recommended Solder Pads

8 Production and packaging information

This chapter describes information such as the patch process, packaging method, storage conditions of the module, which can help users better preserve and use this module.

8.1 Welding production

8.1.1 Furnace passing method

When the module is mounted, the following points need to be noted during reflow soldering:

◆ If the bottom of the module is double-sided SMT, it is recommended to place the module in the second SMT process;

◆ It is best for the customer's substrate to pass through the reflow oven on the carrier tape during the first SMT placement, and for the second SMT placement, it is also advisable to pass through the reflow oven on the carrier tape as much as possible;

◆ If, for special reasons, it is not possible to place it on the mesh belt for reflow soldering, consider using fixtures for reflow soldering on the track or placing a flat, high-temperature resistant straight template under the PCBA to prevent PCB deformation during reflow soldering, leading to virtual soldering of the module.

8.1.2 Soldering operation guidance

The temperature curve of the PCBA reflow soldering oven is related to the use of solder paste and needs to be adjusted according to the actual solder paste. The data is only suitable for lead-free operations, refer to Figure 8.1 for lead-free reflow soldering operation guidelines.

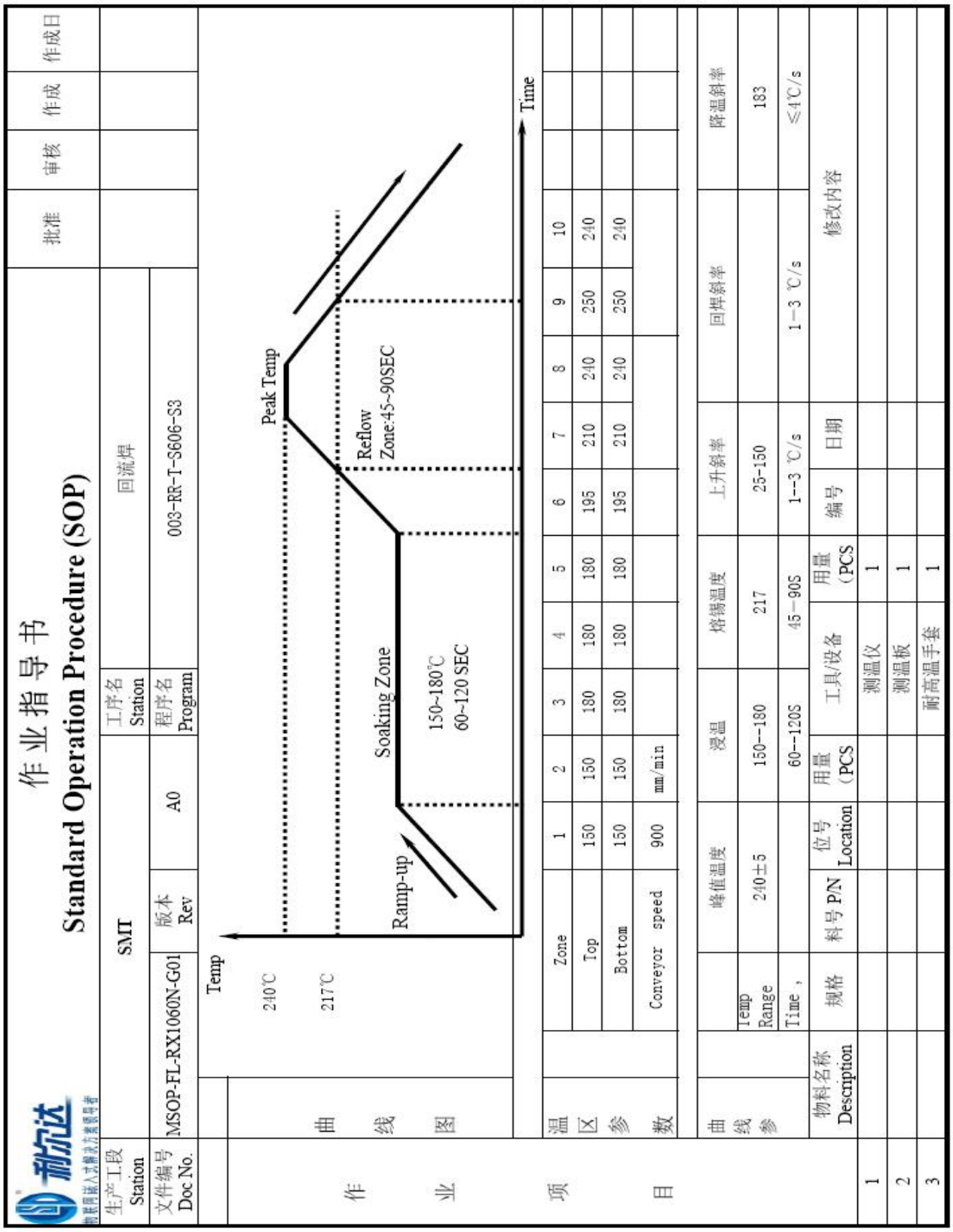


Figure 8.1 Lead-Free Reflow Soldering Operation Guide

8.1.3 Production process

During the production of welding or other processes that may directly contact the module, no organic solvents (such as alcohol, isopropanol, acetone, trichloroethylene, etc.) should be used to wipe the module shield; otherwise, it may cause the shield to rust.

If spraying or potting is required for the module, please ensure that the spraying or potting materials used will not react chemically with the module shield or PCB, and ensure that the spraying or potting materials will not flow into the interior of the module.

8.1.4 Maintenance

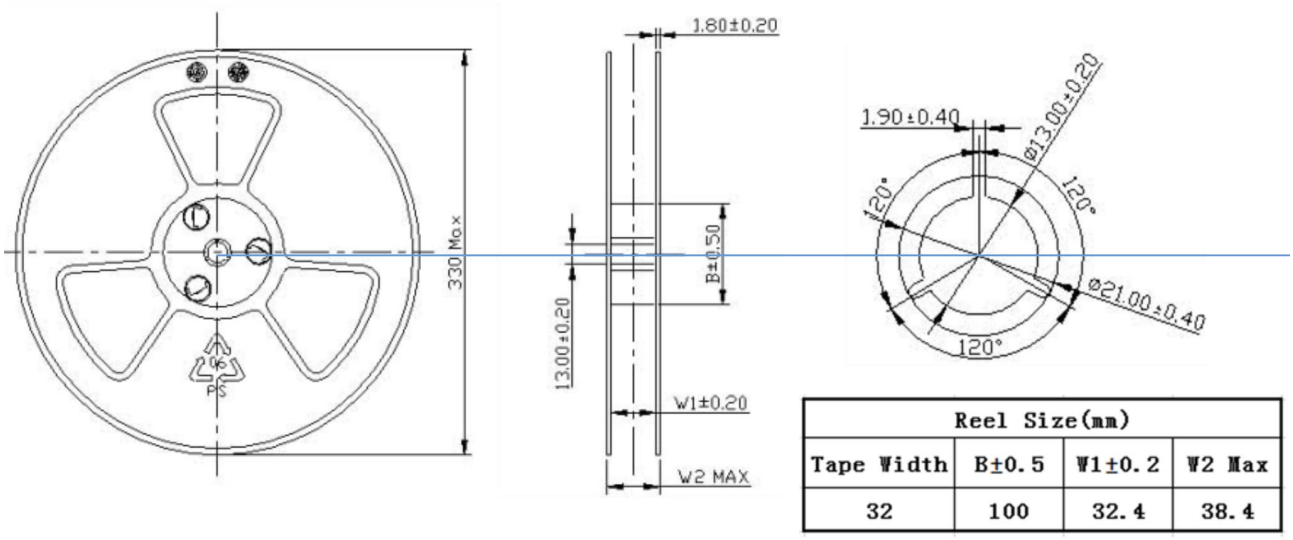
If the module has defects such as virtual welding or short circuit and needs to be repaired, please follow the parameters below:

◆ Lead-free process: Soldering iron temperature 380±10℃, soldering iron contact time ≤5S.

◆ With lead process: Soldering iron temperature 350±10℃, soldering iron contact time ≤5S.

8.2 Packaging specifications

This module uses a rubber wheel carrying method for factory packaging, the reference dimensions of the rubber wheel are as follows:



Reel Size(mm)			
Tape Width	B±0.5	W1±0.2	W2 Max
32	100	32.4	38.4

Figure 8.2 Dimensional drawing of the conveyor belt with rubber wheels

The loading direction of the carrier is as follows: (Refer to the diagram, the label content is subject to the actual situation, pay attention to the position of module PIN1)

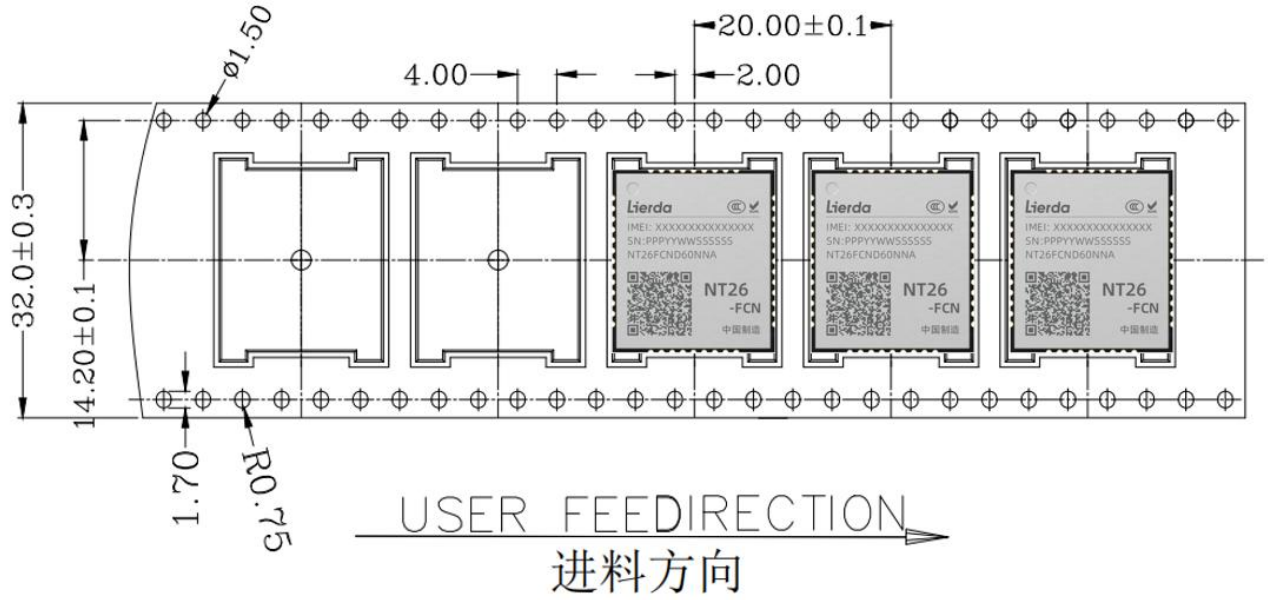


Figure 8.3 Loading direction indicator diagram

8.3 Storage conditions

The module is shipped in the form of a vacuum coiled reel sealed bag, with a humidity

sensitivity level of MSL 3. The storage conditions are as follows:

◆ If the temperature is below 40℃ and the humidity is below 90% (RH), the solderability can be guaranteed for 12 months in well-sealed packaging.

◆ After unpacking, ensure surface mounting assembly within 168 hours under the condition of ambient temperature less than 30℃ and relative humidity less than 60% (RH);

◆ If the above conditions are not met, baking is required. The reel material is baked at 60℃±5℃, humidity ≤60%RH for 48 hours; if accelerated baking is needed, the module needs to be taken out from the reel for individual baking (ESD protection should be observed during the removal process), baked at 125℃±5℃, humidity ≤60%RH for 8 hours, with a total baking time of less than 96 hours.

Please refer to the IPC/JEDEC J-STD-033 standard for more detailed guidance.

9 Related documents and terminology abbreviations

9.1 Related documents

Reference documents are as follows:

Table 9-1 Related Documents

Serial number	Document name	Comment
[1]	IPC/JEDEC J-STD-033 specification	
[2]	Lierda NT26-FEU D Series Hardware Reference Design Manual	

9.2 Term abbreviation

The abbreviations and their corresponding explanations mentioned in this document are as follows:

Table 9-2 Term Abbreviations

Abbreviation	Full English name	Chinese full name
3GPP	3rd Generation Partnership Project	Third Generation Partnership Project
ADC	Analog-to-Digital Converter	Analog-to-digital conversion
ANT	Antenna	Antenna
ASM	Antenna Switch Module	Antenna switch module
DAC	Digital -to- Analog Converter	Analog-to-digital conversion
DBG	Debug	Debugging
DC-DC	Direct Current - Direct Current	DC converter
DCXO	Digitally Controlled Crystal Oscillator	Digital Controlled Crystal

		Oscillator
DRX	Discontinuous Reception	Non-continuous reception
DTE	Data Terminal Equipment	Data terminal equipment
ECL	Equivalent Class Level	Network coverage level
ESD	Electro-Static discharge	Electrostatic discharge
EOS	Electrical Overtress	Electrical super stress (surge)
ESR	Equivalent Series Resistance	Equivalent series resistance
EVK	Evaluation Kit	Evaluate toolkits
H-FDD	Half Frequency Division Duplexing	Frequency Division Half Duplex
FOTA	Firmware Over-The-Air	Remote firmware upgrade
GPIO	General-purpose input/output	Common input and output
I/O	Input/Output	Input and output interface
Imax	Maximum Load Current	Maximum current
Inorm	Normal Current	Normal (typical) current
bps	Bits Per Second	Rate unit
LCC	Leadless Chip Carriers	Leadless chip carrier packaging
LCM	LCD Module	LCD display module
LDO	Low Dropout Regulator	Low dropout linear regulator
LGA	Land Grid Array	Grid array package
LwM2M	Lightweight Machine-To-Machine	Lightweight M2M protocol
MCU	Mirco Controller Unit	Microcontroller
MSL	Moisture Sentivity levels	Humidity sensitivity level
PCB	Printed Circuit Board	Printed Circuit Board
PCBA	Printed Circuit Board Assembly	Printed circuit board components

PMU	Power Management Unit	Power Management Unit
PSM	Power Saving Mode	Energy-saving mode
RF	Radio Frequency	RF
RoHS	Restriction of Hazardous Substances	Limitation of harmful substances
RX	Receive	Receive
TAU	Tracking Area Update	Tracking area update
TCP/IP	Transmission Control Protocol/Internet Protocol	Transmission Control Protocol/Internet Protocol
TVS	Transient Voltage Suppressor	Transient Voltage Suppression Diode
TX	Transmit	Send
UART	Universal Asynchronous Receiver & Transmitter	General asynchronous receiver and transmitter
UDP/IP	User Datagram Protocol - Internet Protocol	User Datagram Protocol
URC	Unsolicited Result Code	Non-request result code
(U)SIM	(Universal) Subscriber Identification Module	Universal user identity recognition module
VSWR	Voltage Standing Wave Ratio	Voltage Standing Wave Ratio
Vmax	Maximum Voltage Value	Maximum voltage
Vnorm	Normal Voltage Value	Normal (typical) voltage
Vmin	Minimum Voltage Value	Minimum voltage
VIHmax	Maximum Input High Level Voltage Value	Maximum input high level
VIHmin	Minimum Input High Level Voltage Value	Minimum input high level
VILmax	Maximum Input Low Level Voltage Value	Maximum input low level
VILmin	Minimum Input Low Level Voltage Value	Minimum input low level
VImax	Absolute Maximum Input Voltage Value	Maximum input level
VImin	Absolute Minimum Input Voltage Value	Minimum input level

VOHmax	Maximum Output High Level Voltage Value	Maximum output high level
VOHmin	Minimum Output High Level Voltage Value	Minimum output high level
VOLmax	Maximum Output Low Level Voltage Value	Maximum output low level
VOLmin	Minimum Output Low Level Voltage Value	Minimum output low level